LG Semicon

MOS MEMORY V

DATA BOOK

■ SDRAM

■ Product Status

DEFINITIONS		
Data Sheet Indentification	**Product Status**	**Definition**
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. LG Semicon CO., Ltd. reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. LG Semicon CO., Ltd. reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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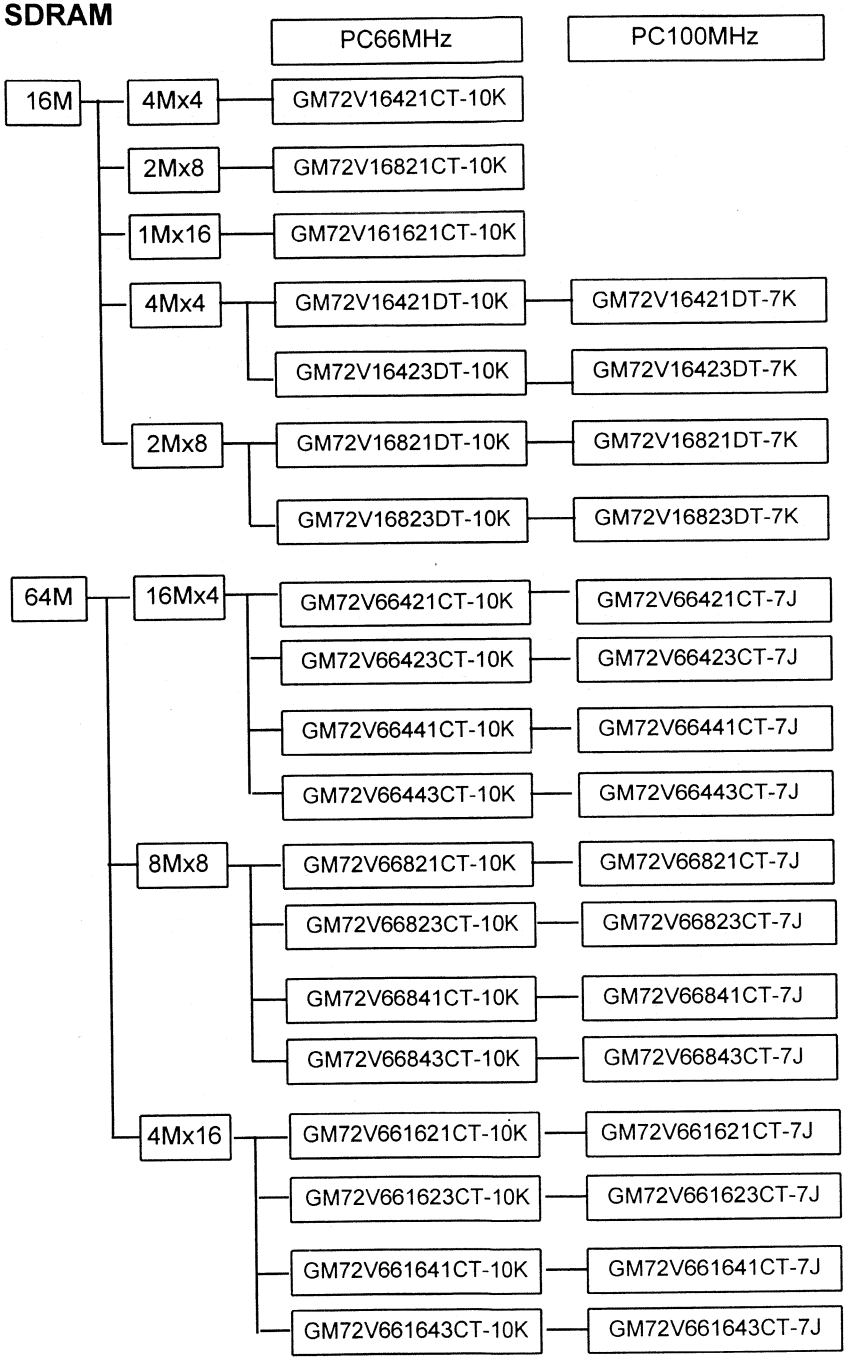
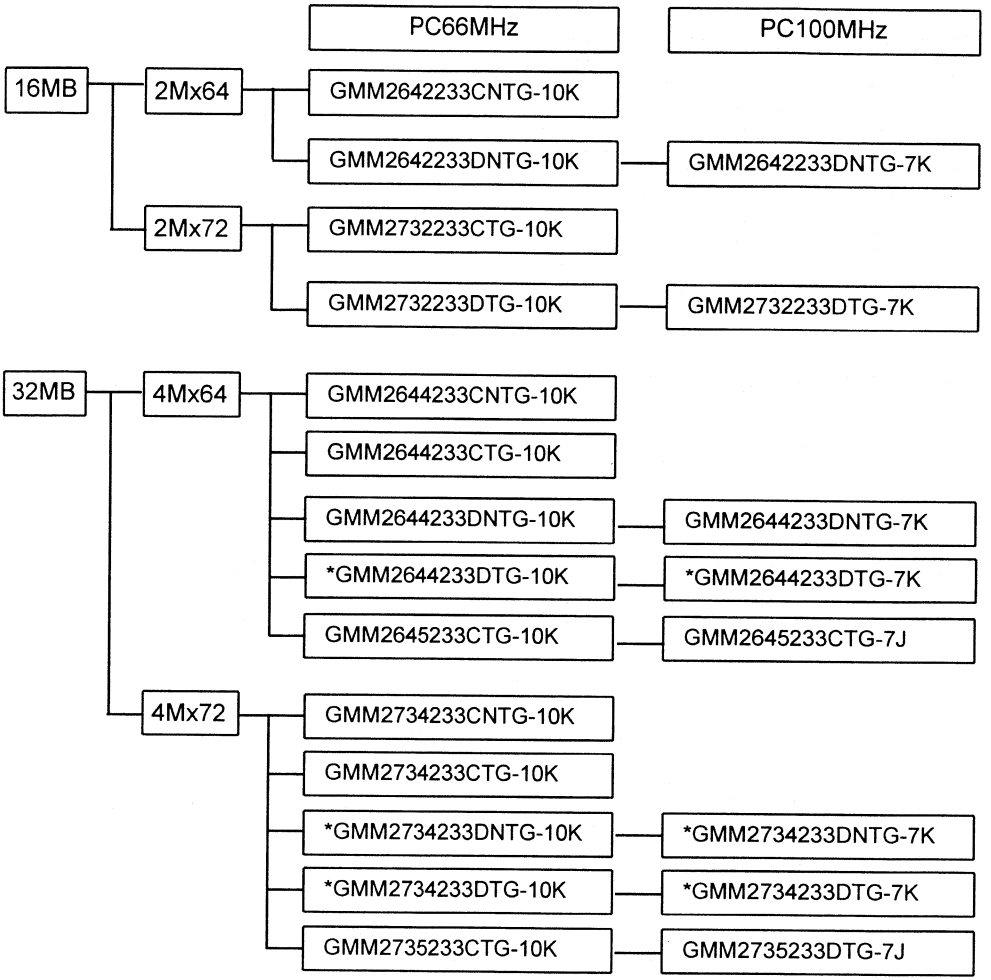


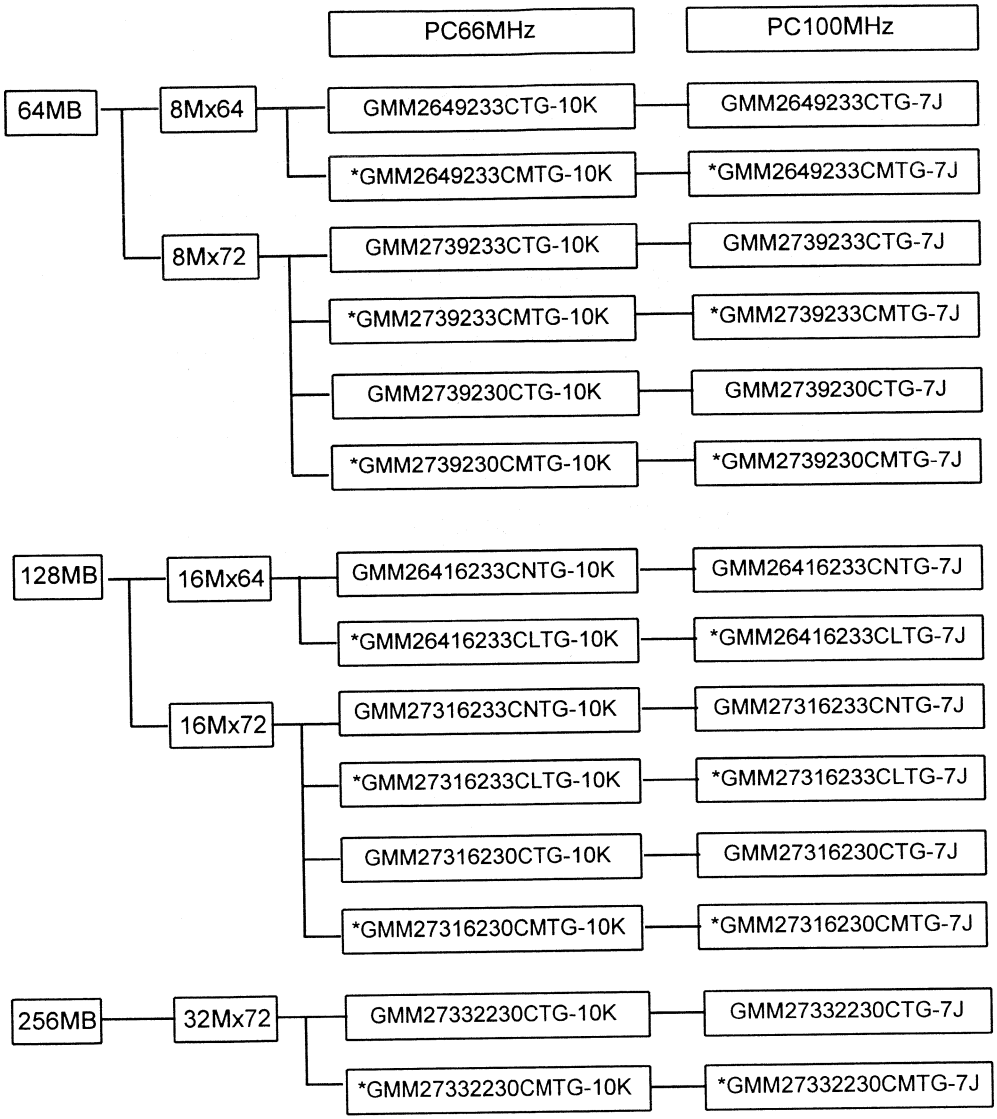
NOTE : * ; Comming Soon, † ; Under Development

2. SDRAM DIMM MODULE



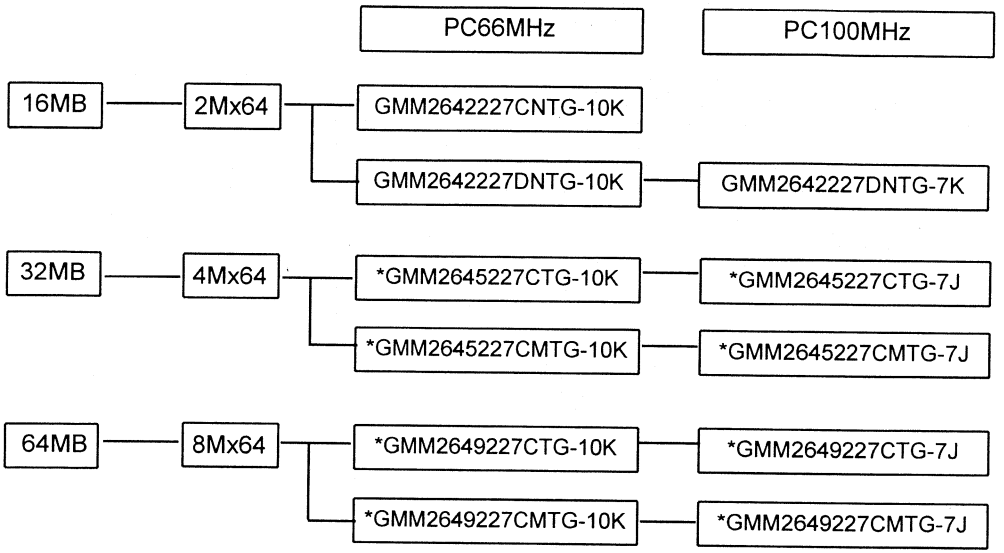
NOTE : * ; Comming Soon, † ; Under Development

SDRAM DIMM MODULE (Contiuned)



NOTE : * ; Comming Soon, † ; Under Development

3. SDRAM SODIMM MODULE



NOTE : * ; Comming Soon, † ; Under Development

SDRAM

Org.	Part Number	Volt.	Speed	Ref.	Mode	PACKAGE	AVAIL.
2M x 4 x2 Bank	GM72V16421CT	3.3V	66/83/100 MHz	4K	LVTTL	44 TSOP II (400MIL)	NOW
1M x 8 x 2 Bank	GM72V16821CT				LVTTL		
2M x 4 x 2 Bank	GM72V16421DT		100/133 MHz		LVTTL	44 TSOP II (400MIL)	NOW
1M x 8 x 2 Bank	GM72V16821DT				SSTL-3		
512K x 16 x 2 Bank	GM72V161621CT		66/83/100 MHz		SSTL-3	50 TSOP II (400MIL)	
8M x 4 x2 Bank	GM72V66421CT	3.3V	66/83/100 MHz	4K	LVTTL	54 TSOP II (400MIL)	NOW
	GM72V66423CT				SSTL-3		
4M x 4 x4 Bank	GM72V66441CT				LVTTL		
	GM72V66443CT				SSTL-3		
4M x 8 x2 Bank	GM72V66821CT				LVTTL		
	GM72V66823CT				SSTL-3		
2M x 8 x4 Bank	GM72V66841CT				LVTTL		
	GM72V66843CT				SSTL-3		
2M x 16 x2 Bank	GM72V661621CT				LVTTL		
	GM72V661623CT				SSTL-3		
1M x 16 x4 Bank	GM72V661641CT				LVTTL		
	GM72V661643CT				SSTL-3		

*NOTE

LVTTL : Low Voltage Transistor Transistor Logic
CTT : Center Tapped Termination
SSTL-3 : Stub Series -Terminated Transceiver Logic

• 16M Byte SDRAM Module (168 pin DIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
2M x64	GMM2642233CNTG	(2Mx8) x 8	3.3V	66/83/100MHz	4K	NOW	Non-Parity
	GMM2642233DNTG			100/133MHz			
2M x72	GMM2732233CTG	(2Mx8) x 9		66/83/100MHz			ECC
	GMM2732233DTG			100/133MHz			

• 32M Byte SDRAM Module (168 pin DIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
4M x64	GMM2644233CNTG	(2Mx8) x 16	3.3V	66/83/100MHz	4K	NOW	Non-Parity
	GMM2644233DNTG			100/133MHz			
	GMM2644233CTG	(4Mx4) x 16		66/83/100MHz			
	GMM2644233DTG			100/133MHz		MAR98	
	GMM2645233CTG	(4Mx16) x 4		100/125MHz		NOW	
4M x72	GMM2734233CNTG	(2Mx8) x 18		66/83/100MHz			ECC
	GMM2734233DNTG			100/133MHz		MAR98	
	GMM2734233CTG	(4Mx4) x 18		66/83/100MHz		NOW	
	GMM2734233DTG			100/133MHz		MAR98	
	GMM2735233CTG	(4Mx16) x 5		100/125MHz		NOW	

• 64M Byte SDRAM Module (168 pin DIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
8M x64	GMM2642233CTG	(8Mx8) x 8	3.3V	100/125MHz	4K	NOW	Non-Parity
	GMM2642233CMTG					MAR98	
8M x72	GMM2739233CTG	(8Mx8) x 9				NOW	ECC
	GMM2739233CMTG					MAR98	
	GMM2739230CTG					NOW	
	GMM2739230CMTG					MAR98	

• 128M Byte SDRAM Module (168 pin DIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
16M x64	GMM26416233CNTG	(8Mx8) x 16	3.3V	100/125MHz	4K	NOW	Non-Parity
	GMM26416233CLTG					MAR98	
16M x72	GMM27391633CNTG	(8Mx8) x 18				NOW	ECC
	GMM27391633CLTG					MAR98	
	GMM27316230CTG	(16Mx4) x 18				NOW	
	GMM27316230CMTG					MAR98	

• 256M Byte SDRAM Module (168 pin DIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
32M x72	GMM27332233CTG	(16Mx4) x 36	3.3V	100/125MHz	4K	NOW	ECC
	GMM27332230CMTG					MAR98	

• 16M Byte SDRAM Module (144pin SODIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
2M x64	GMM2642227CNTG	(2Mx8) x 8	3.3V	66/83/100MHz	4K	NOW	ECC
	GMM2642227DNTG			100/133MHz			

• 32M Byte SDRAM Module (144pin SODIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
4M x64	GMM2645227CTG	(4Mx16) x 4	3.3V	100/125MHz	4K	MAR98	ECC
	GMM2645227CMTG						

• 64M Byte SDRAM Module (144pin SODIMM)

Org.	Part Number	Composition	Volt.	Speed (ns)	Feature	Avail.	Remark
8M x64	GMM2649227CTG	(8Mx8) x 8	3.3V	100/125MHz	4K	MAR98	ECC
	GMM2649227CMTG						

A. TERMS AND DEFINITION

VOLTAGES

V_{IH} High-level input voltage

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits guaranteed.

V_{IL} Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits guaranteed.

V_{OH} High-level output voltage

The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage

The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

V_{DD} Supply voltage (V_{CC}, V_{PP})

The voltage supplied to the corresponding voltage pins that are required for the device to the function.

CURRENT

I_{IH} High-level input current

The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current

The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current

The current flowing* the output with a specified high-level output voltage V_{OH} applied.

I_{OL} Low-level output current

The current flowing* the output with a specified low-level output voltage V_{OL} applied.

*Note: The current flowing out of a terminal is a negative value.

$I_{O(off)}$ Off-state output current

The current flowing into* an output with a specified output applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

*Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current

The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CC}, I_{DD} Supply current

The current into, respectively, the V_{DD}, V_{CC} supply terminal.

DYNAMIC CHARACTERISTICS

t_A Access Time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

(Example)

t_{ACC} : Address access time

t_{ACS} : Chip select access time

t_{OE} : Output enable access time

t_{RC} Cycle Time

The time interval between the start and end of a cycle.

(Example)

t_{RC} : Read cycle time

t_{WC} : Write cycle time

t_{SU} Setup Time

The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

(Example)

t_{AS} : Address set-up time

t_{DW} : Input data set-up time

t_{ASW} : Write address set-up time

t_{HOLD} Hold Time

The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

(Example)

t_{RAH} : Row address hold time

t_{DH} : Input data hold time

t_{ROH} : Output data hold time from $\overline{RAS}$

t_W Pulse Duration (width)

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

(Example)

t_{WP} : Write pulse duration

t_{SP} : Chip select pulse width

t_{REF} Refresh time interval

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital is guaranteed.

(Example)

t_{REF} : Refresh time interval

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same wave form that is changing form the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Valid time

(a) General

The time interval during which a signal is (or should be) valid.

(b) Output data-valid time

The time interval in which output data continues to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Enable time (of a three-state output)

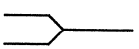
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

*Note: For memories these intervals are often classified as access times.

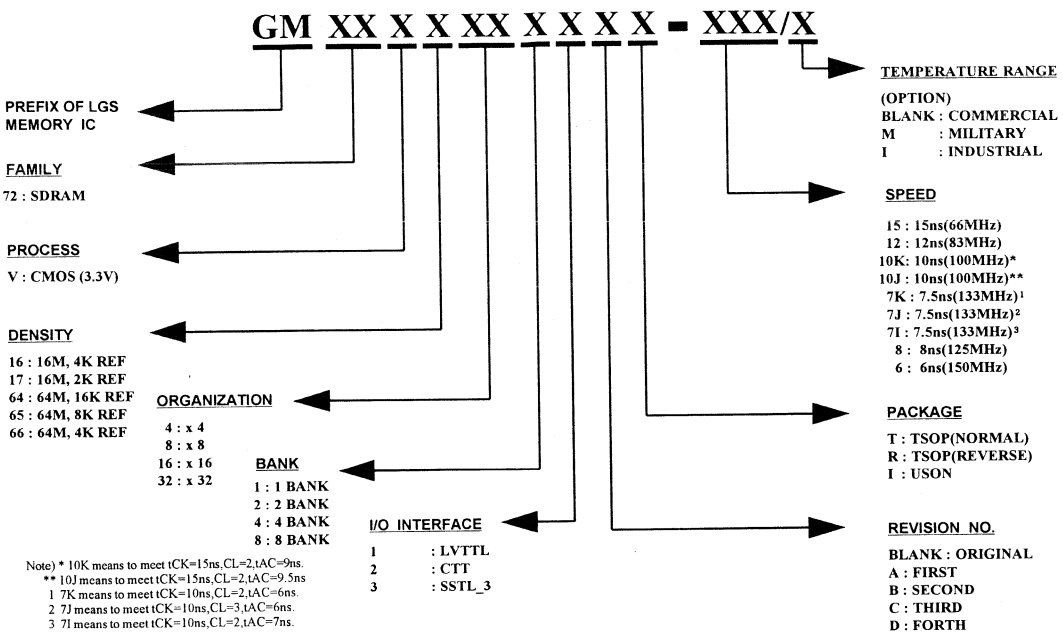
Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

B. WAVEFORMS

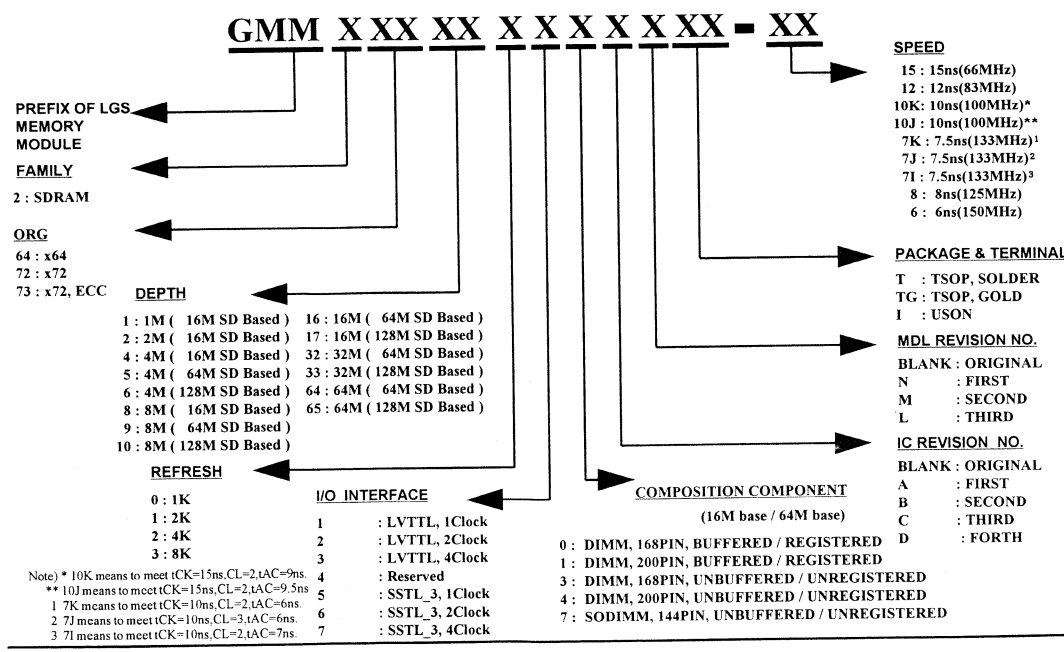
Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM 'H' TO 'L'	WILL CHANGE FROM 'H' TO 'L'
	CHANGE FROM 'L' TO 'H'	WILL CHANGE FROM 'L' TO 'H'
	DON'T CARE : ANY CHANGE PERMITTED	CHANGING : STATE UNKNOWN
	N/A	HIGH IMPEDANCE

SDRAM ORDERING INFORMATION(16M & 64M SDRAM)



Note) * 10K means to meet tCK=15ns,CL=2,tAC=9ns.
** 10J means to meet tCK=15ns,CL=2,tAC=9.5ns
1 7K means to meet tCK=10ns,CL=2,tAC=6ns.
2 7J means to meet tCK=10ns,CL=3,tAC=6ns.
3 7I means to meet tCK=10ns,CL=2,tAC=7ns.

SDRAM MODULE ORDERING INFORMATION (16M / 64M SD BASE)



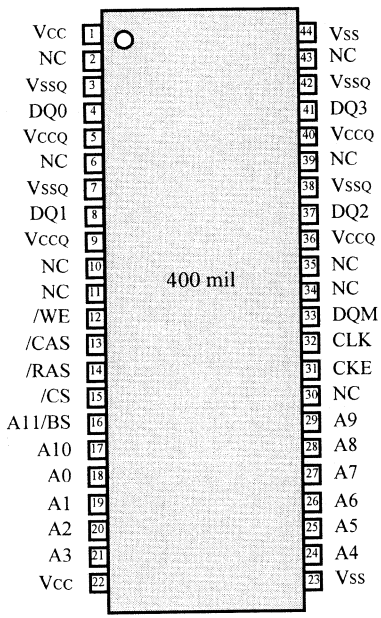
Note) * 10K means to meet tCK=15ns,CL=2,tAC=9ns.
** 10J means to meet tCK=15ns,CL=2,tAC=9.5ns
1 7K means to meet tCK=10ns,CL=2,tAC=6ns.
2 7J means to meet tCK=10ns,CL=3,tAC=6ns.
3 7I means to meet tCK=10ns,CL=2,tAC=7ns.

Description

The GM72V16421CT is new generation synchronous dynamic RAM, organized 2,097,152 words x 4bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 44pin 400mil plastic TSOP II.

Pin Configuration

44 TSOP II



(Top View)

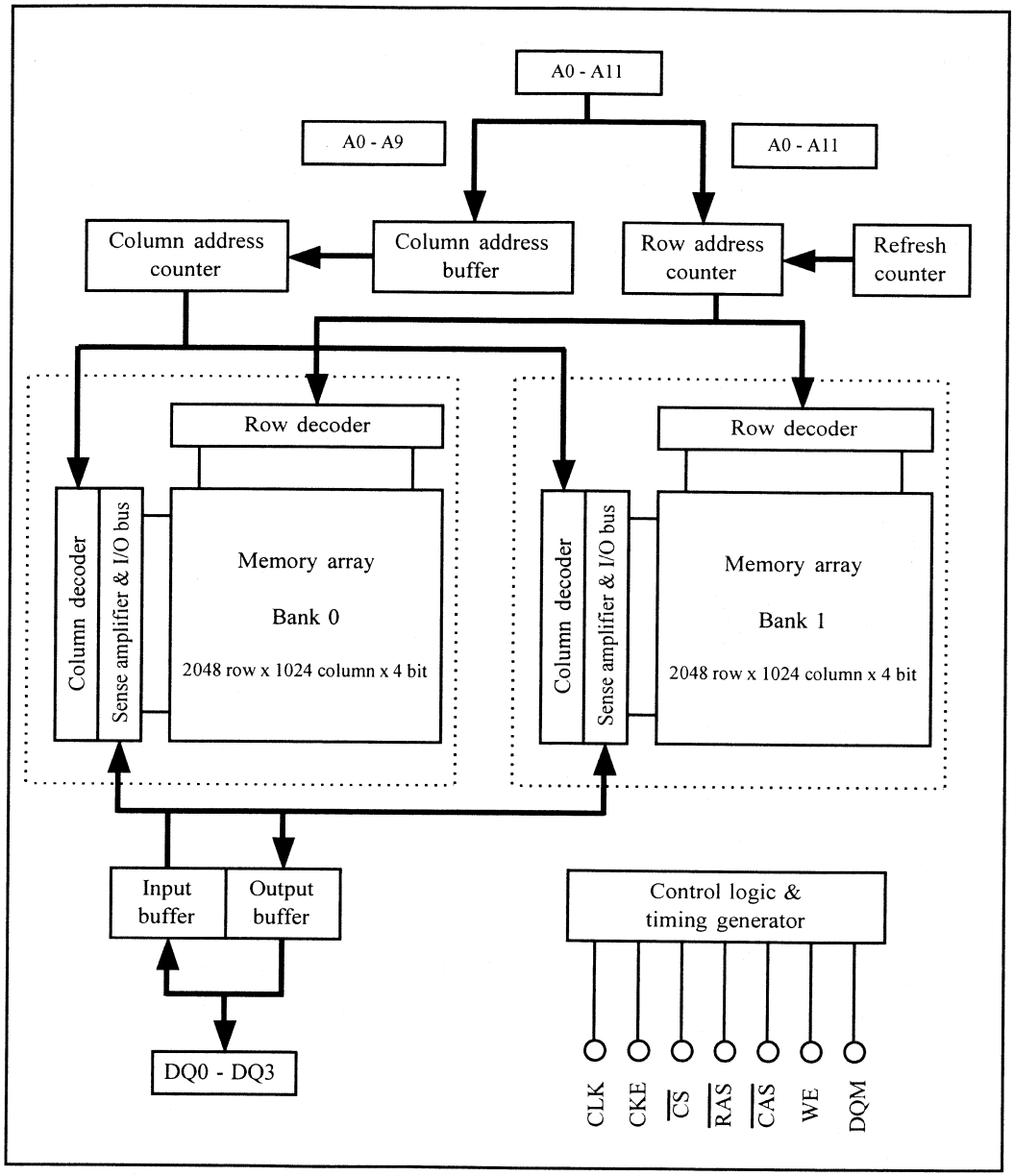
Features

- 2,097,152 Words x 4 Bit x 2 Bank Organization
- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- 2 Bank can operate simultaneously and independently
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- 44Pin 400mil TSOP II Package

Pin Name

CLK	CLocK input
$\overline{CKE}$	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ3	Data input / output
DQM	Data input / output Mask
VCCQ	Power for DQ circuit (3.3V)
VSSQ	Power for DQ circuit
VCC	Power for internal circuit (3.3V)
VSS	Ground for internal circuit
NC	No Connection

Block Diagram(GM72V16421CT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A9 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V16421CT Series is divided into bank 0 and bank 1. GM72V16421CT Series contain 2048 row x 1024 column x 4bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ3 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQM (input pins)	DQM controls input/output buffers. • Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. • Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0~A9
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST]:** This command stops a full-page burst operation (burst length = 1024), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY9) and the bank select address (A11). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY9) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY9) and the bank select address (A11).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11(BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self -refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

The GM72V16421CT series can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V16421CT operating instructions.

CKE Truth Table

Current State	Function	CKE n -1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh REF command	H	H	L	L	L	H	X
Idle	Self-refresh SELF entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh SELFX exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.

2. An interval of t_{RWL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		-15		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	100	-	85	-	70	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	3	-	3	-	3	mA	CKE=V_{IL}, t_{CK}=min	5
			-	2	-	2	-	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	40	-	35	-	30	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
Active standby current (Bank Active)		I_{CC3}	-	7	-	7	-	7	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
			-	45	-	40	-	35	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
Burst operating current	(CL=1)	I_{CC4}	-	65	-	55	-	45	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)	I_{CC4}	-	100	-	85	-	65	mA		
	(CL=3)	I_{CC4}	-	150	-	125	-	100	mA		
Refresh current		I_{CC5}	-	85	-	70	-	60	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	-	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3
Output capacitance (I/O)	C_O	-	7	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-10		-12		-15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	45	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-	22.5	-		
	(CL=3)	t_{CK}	10	-	12	-	15	-		
CLK high pulse width		t_{CKH}	3	-	4	-	5	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	5	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	-	36	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12	-	17		
	(CL=3)	t_{AC}	-	7.5	-	9	-	12		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	13	-	15	-	17	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9	-	11		
Data-in setup time		t_{DS}	2	-	3	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	3	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	3	-	3	-	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		- 15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CKE hold time	t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	100	-	135	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	70	120000	90	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	30	-	45	-	ns	1
Precharge to active command period	t_{RP}	30	-	30	-	45	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	15	-	22.5	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	20	-	30	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

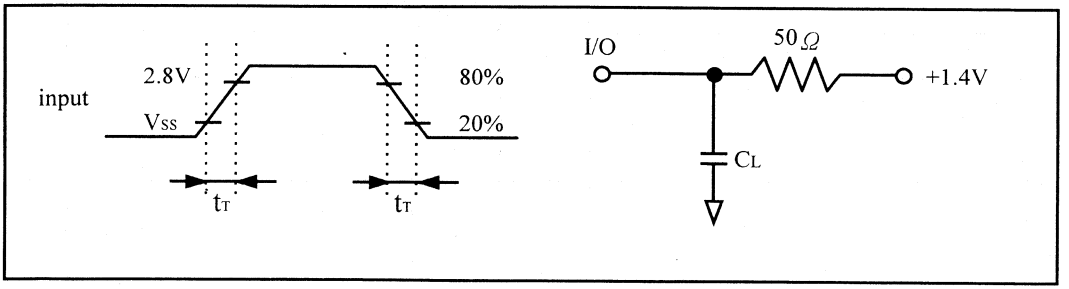
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-10			-12			-15			Notes
			100	66	33	83	55	28	66	44	22	
			10	15	30	12	18	36	15	22.5	45	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	3	2	1	1
Last data input to Precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

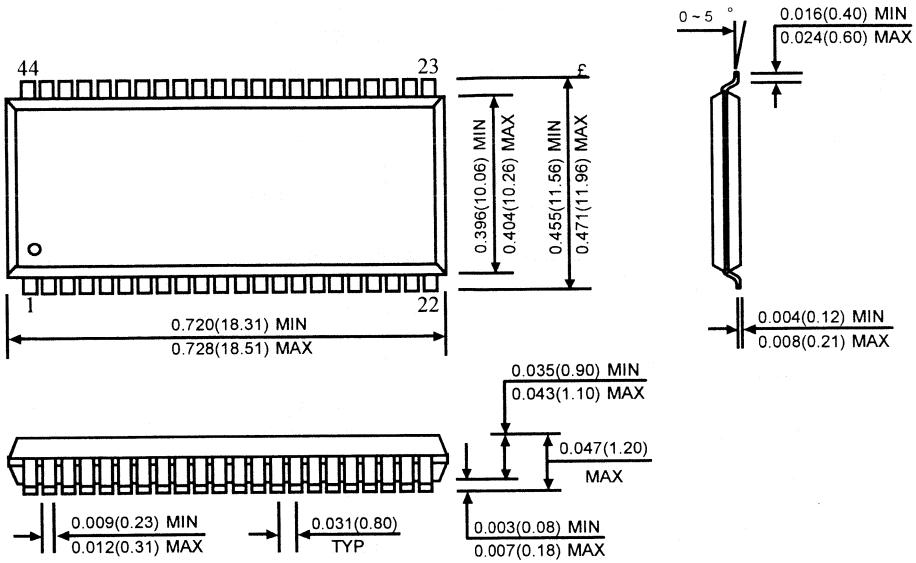
Parameter		Symbol	- 10			- 12			- 15			Notes
Frequency (MHz)			100	66	33	83	55	28	66	44	22	
t_{CK} (ns)			10	15	30	12	18	36	15	22.5	45	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

Unit: Inches (mm)

44 TSOP II



LG Semicon Co.,Ltd.

GM72V16421DT

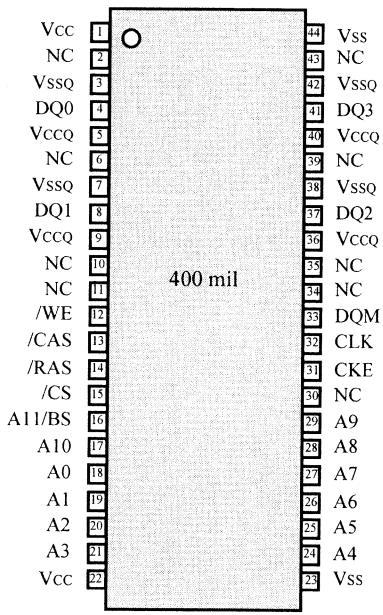
2,097,152 WORDS x 4BIT x 2BANK
SYNCHRONOUS DYNAMIC RAM

Description

The GM72V16421DT is new generation synchronous dynamic RAM, organized 2,097,152 words x 4bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 44pin 400mil plastic TSOP II.

Pin Configuration

44 TSOP II



(Top View)

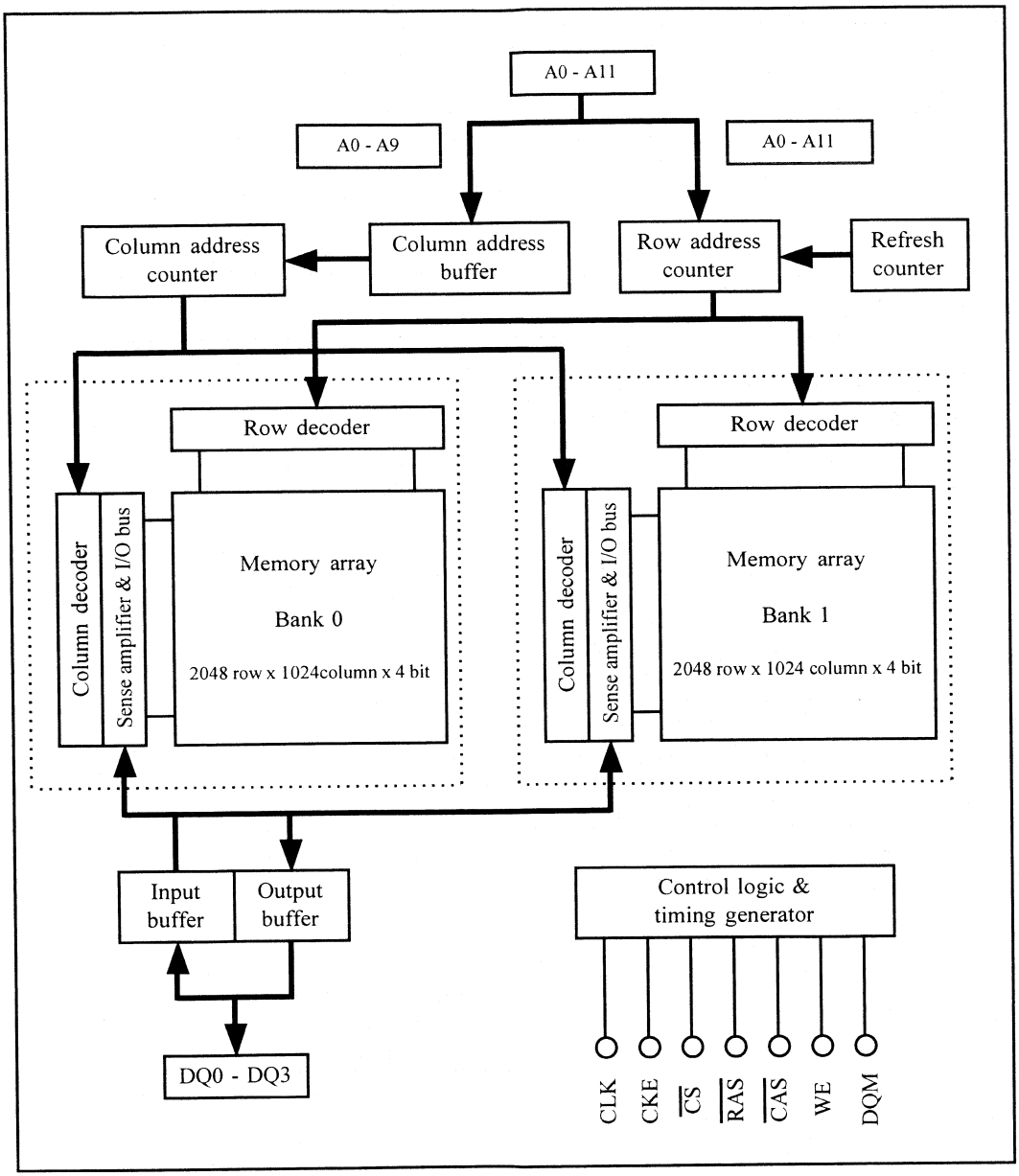
Features

- 2,097,152 Words x 4 Bit x 2 Bank Organization
- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  83 / 100 / 133 MHz
- LVTTL Interface
- 2 Bank can operate simultaneously and independently
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- 44Pin 400mil TSOP II Package

Pin Name

CLK	CLocK input
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ3	Data input / output
DQM	Data input / output Mask
VCCQ	Power for DQ circuit (3.3V)
VSSQ	Power for DQ circuit
VCC	Power for internal circuit (3.3V)
VSS	Ground for internal circuit
NC	No Connection

Block Diagram(GM72V16421DT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A9 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V16421DT Series is divided into bank 0 and bank 1. GM72V16421DT Series contain 2048 row x 1024 column x 4bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ3 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQM (input pins)	DQM controls input/output buffers. • Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. • Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0~A9
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST]:** This command stops a full-page burst operation (burst length = 1024), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY9) and the bank select address (A11). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY9) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY9) and the bank select address (A11).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11(BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self -refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

The GM72V16421DT series can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V16421DT operating instructions.

CKE Truth Table

Current State	Function	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh command REF	H	H	L	L	L	H	X
Idle	Self-refresh entry SELF	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: VIH, L: VIL, X: VIH or VIL.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	Other bank READ/READA ILLEGAL on same bank
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Other bank WRIT/WRIT A ILLEGAL on same bank
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	Other bank READ/READA ILLEGAL on same bank
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Other bank WRIT/WRIT A ILLEGAL on same bank
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.

2. An interval of t_{RWL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start and the currently READA bank precharge is automatically performed. (Attempting to make the currently READA bank READ/READA results in an illegal command.)

To [WRIT], [WRIT A]: These commands stop a burst read, and start a WRIT/WRITA cycle and the currently READA bank precharge is automatically performed. (Attempting to make the currently READA bank WRIT/WRITA results in an illegal command.)

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

To [READ], [READ A]: These commands stop a burst write and start a READ/READA cycle and the currently WRITA bank precharge is automatically performed. (Attempting to make the currently WRITA bank READ/READA results in an illegal command.)

To [WRIT], [WRIT A]: These commands stop a burst write, and start a WRIT/WRITA cycle. The currently WRITA bank precharge is automatically performed. (Attempting to make the currently WRITA bank WRIT / WRITA results in an illegal command.)

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter	Symbol	-75		-10		-12		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	-	100	-	100	-	85	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	-	2	-	3	-	3	mA	CKE=V_{IL}, t_{CK}=min	5
	I_{CC2}	-	2	-	2	-	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
	(100MHz)	-	40	-	40	-	35	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
	(133MHz)	-	55							
Active standby current (Bank Active)	I_{CC3}	-	7	-	7	-	7	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
	(100MHz)	-	45	-	45	-	40	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
	(133MHz)	-	60							
Burst operating current (CL=1)	I_{CC4}	-	-	-	65	-	55	mA	t_{CK}=min BL = 4	1, 2, 4
Burst operating current (CL=2)		-	150	-	100	-	85	mA		
Burst operating current (CL=3)		-	190	-	150	-	125	mA		
Refresh current	I_{CC5}	-	85	-	85	-	70	mA	t_{RC}=min	
Self refresh current	I_{CC6}	-	0.4	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	0 ≤ Vout ≤ V_{CC} I/O = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)
(GM72V16421DT-10/12)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	2	5	pF	1, 3
Output capacitance (I/O)	C_O	4	7	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)
(GM72V16421DT-75)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2.5	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	2.5	4	pF	1, 3
Output capacitance (I/O)	C_O	4	6.5	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 75		- 10		- 12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9.5	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

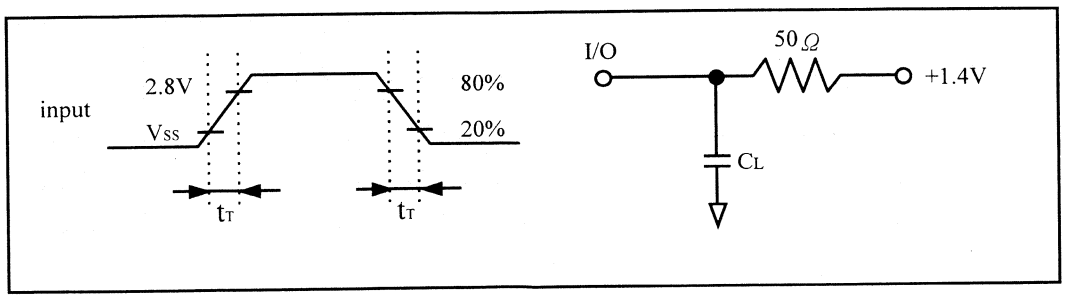
Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.
6. -10 grade products are classified as follows.
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.
   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.
   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

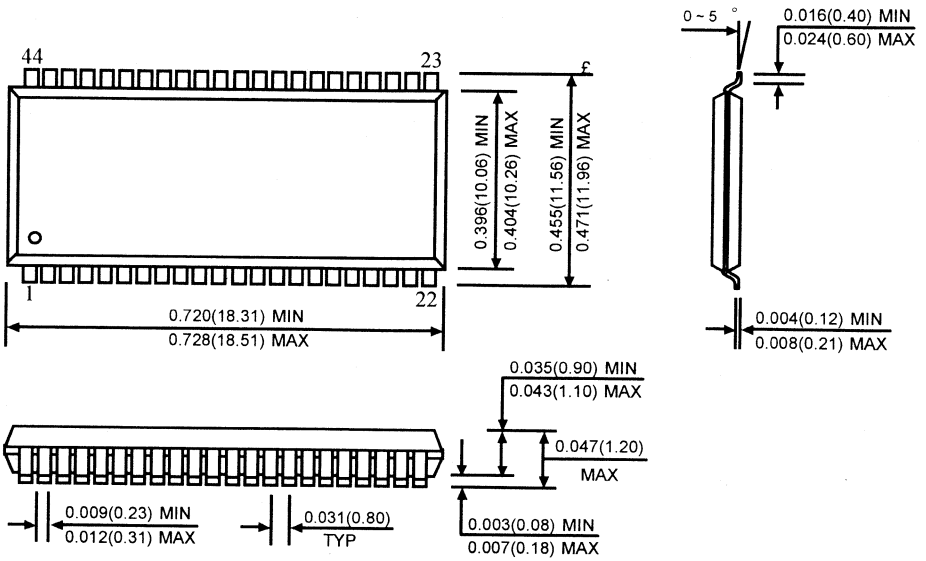
Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

Unit: Inches (mm)

44 TSOP II



GM72V16821CT

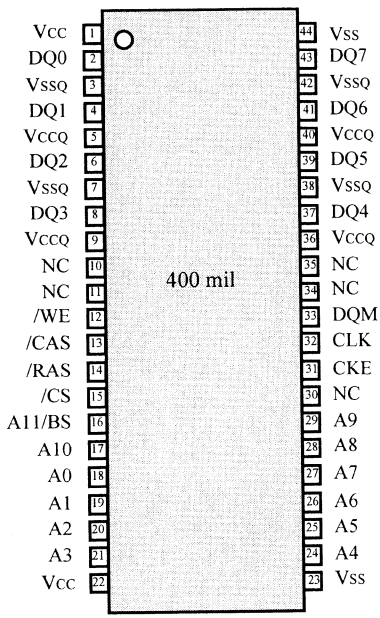
1,048,576 WORDS x 8BIT x 2BANK
SYNCHRONOUS DYNAMIC RAM

Description

The GM72V16821CT is new generation synchronous dynamic RAM, organized 1,048,576 words x 8bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 44pin 400mil plastic TSOP II.

Pin Configuration

44 TSOP II



(Top View)

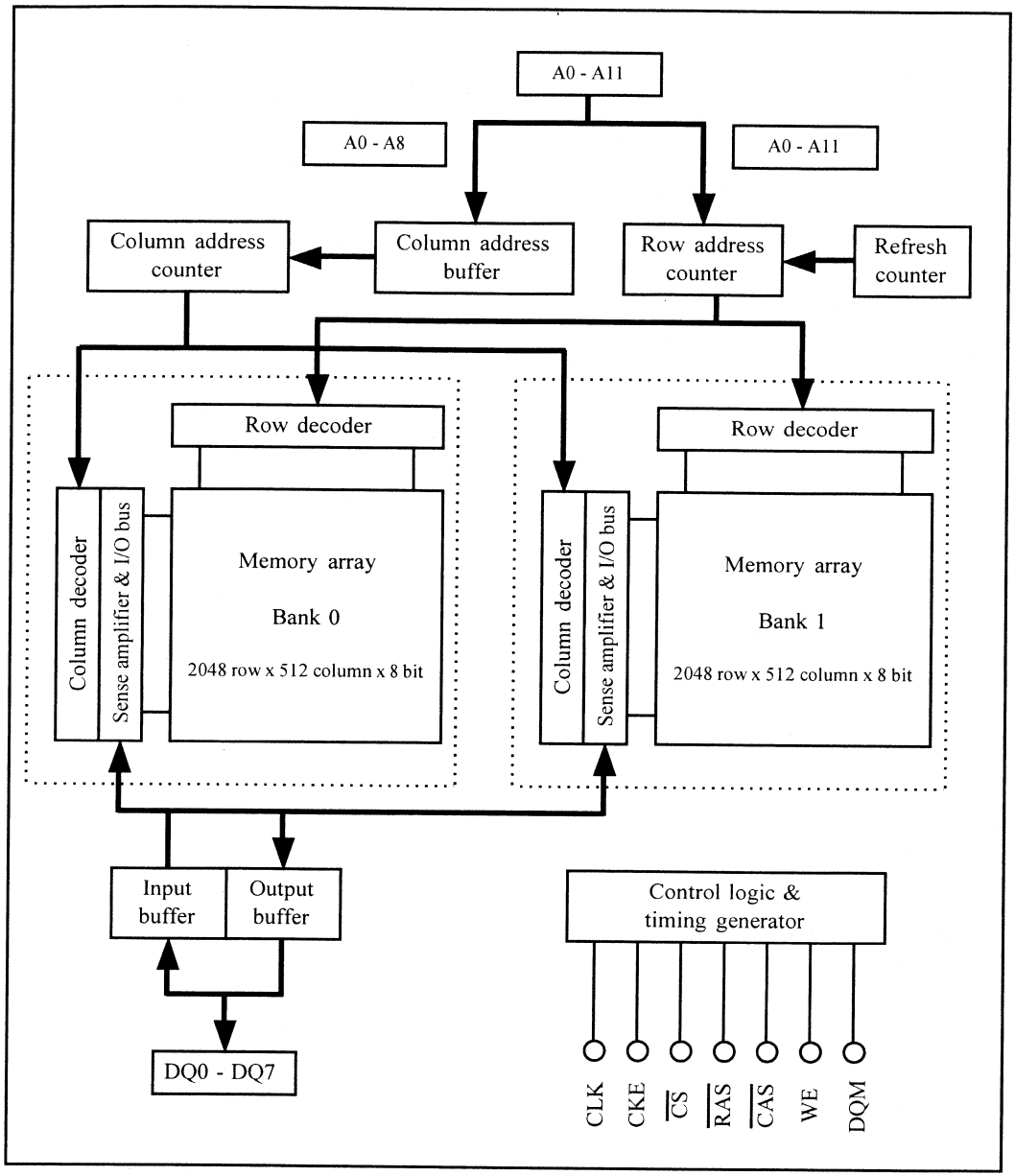
Features

- 1,048,576 Words x 8 Bit x 2 Bank Organization
- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- 2 Bank can operate simultaneously and independently
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- 44Pin 400mil TSOP II Package

Pin Name

CLK	CLocK input
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ7	Data input / output
DQM	Data input / output Mask
Vccq	Power for DQ circuit (3.3V)
Vssq	Power for DQ circuit
Vcc	Power for internal circuit (3.3V)
Vss	Ground for internal circuit
NC	No Connection

Block Diagram(GM72V16821CT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V16821CT Series is divided into bank 0 and bank 1. GM72V16821CT Series contain 2048 row x 512 column x 8bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQM (input pins)	DQM controls input/output buffers. • Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. • Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0~A9
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST]:** This command stops a full-page burst operation (burst length = 512), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8) and the bank select address (A11). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY8) and the bank select address (A11).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11(BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self -refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

The GM72V16821CT series can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V16821CT operating instructions.

CKE Truth Table

Current State	Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
		n -1	n					
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh REF command	H	H	L	L	L	H	X
Idle	Self-refresh entry SELF	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.

2. An interval of t_{RWL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		-15		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	100	-	85	-	70	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	3	-	3	-	3	mA	CKE=V_{IL}, t_{CK}=min	5
			-	2	-	2	-	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	40	-	35	-	30	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
Active standby current (Bank Active)		I_{CC3}	-	7	-	7	-	7	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
			-	45	-	40	-	35	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
Burst operating current	(CL=1)	I_{CC4}	-	65	-	55	-	45	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)	I_{CC4}	-	100	-	85	-	65	mA		
	(CL=3)	I_{CC4}	-	150	-	125	-	100	mA		
Refresh current		I_{CC5}	-	85	-	70	-	60	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0≤Vin≤V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0≤Vout≤V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	-	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3
Output capacitance (I/O)	C_O	-	7	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		- 15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	45	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-	22.5	-		
	(CL=3)	t_{CK}	10	-	12	-	15	-		
CLK high pulse width		t_{CKH}	3	-	4	-	5	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	5	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	-	36	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12	-	17		
	(CL=3)	t_{AC}	-	7.5	-	9	-	12		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	13	-	15	-	17	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9	-	11		
Data-in setup time		t_{DS}	2	-	3	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	3	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	3	-	3	-	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		- 15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CKE hold time	t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	100	-	135	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	70	120000	90	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	30	-	45	-	ns	1
Precharge to active command period	t_{RP}	30	-	30	-	45	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	15	-	22.5	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	20	-	30	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

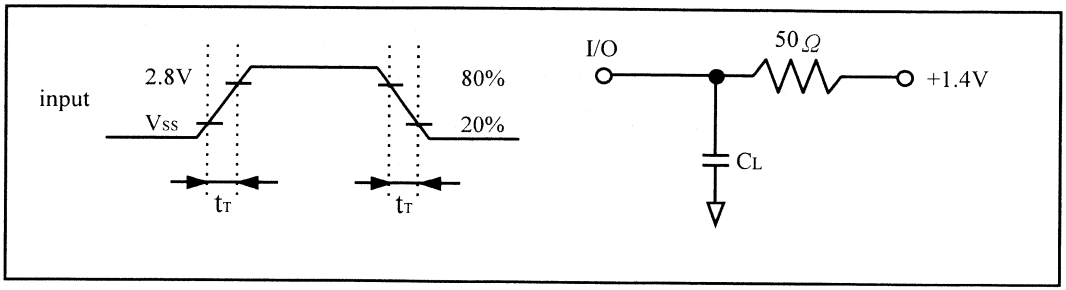
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-10			-12			-15			Notes
			100	66	33	83	55	28	66	44	22	
			10	15	30	12	18	36	15	22.5	45	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	3	2	1	1
Last data input to Precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

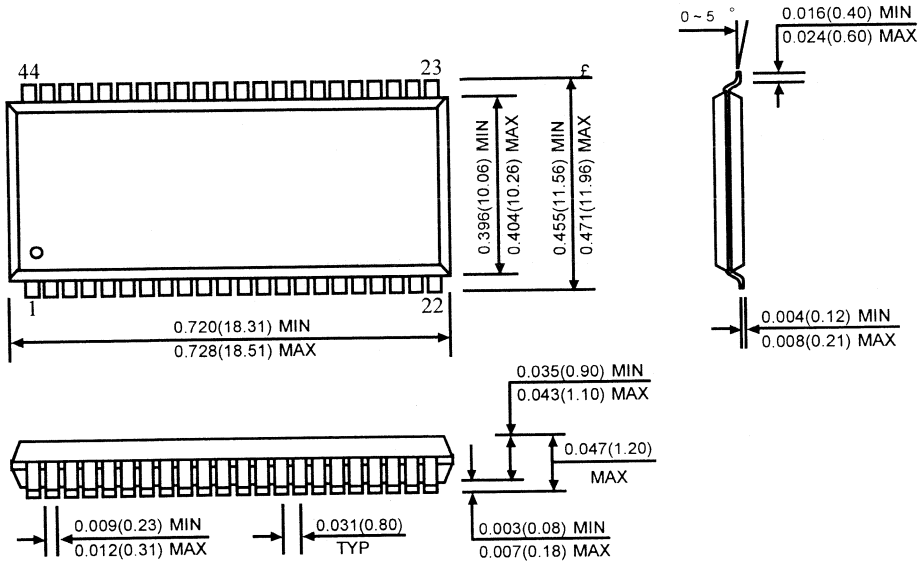
Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-10			-12			-15			Notes
			100	66	33	83	55	28	66	44	22	
			10	15	30	12	18	36	15	22.5	45	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

Unit: Inches (mm)

44 TSOP II



LG Semicon Co.,Ltd.

GM72V16821DT

1,048,576 WORDS x 8BIT x 2BANK
SYNCHRONOUS DYNAMIC RAM

Description

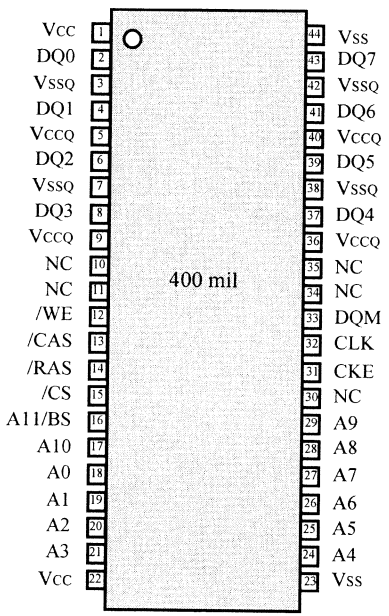
The GM72V16821DT is new generation synchronous dynamic RAM, organized 1,048,576 words x 8bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 44pin 400mil plastic TSOP II.

Features

- 1,048,576 Words x 8 Bit x 2 Bank Organization
- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  83 / 100 / 133 MHz
- LVTTL Interface
- 2 Bank can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- 44Pin 400mil TSOP II Package

Pin Configuration

44 TSOP II

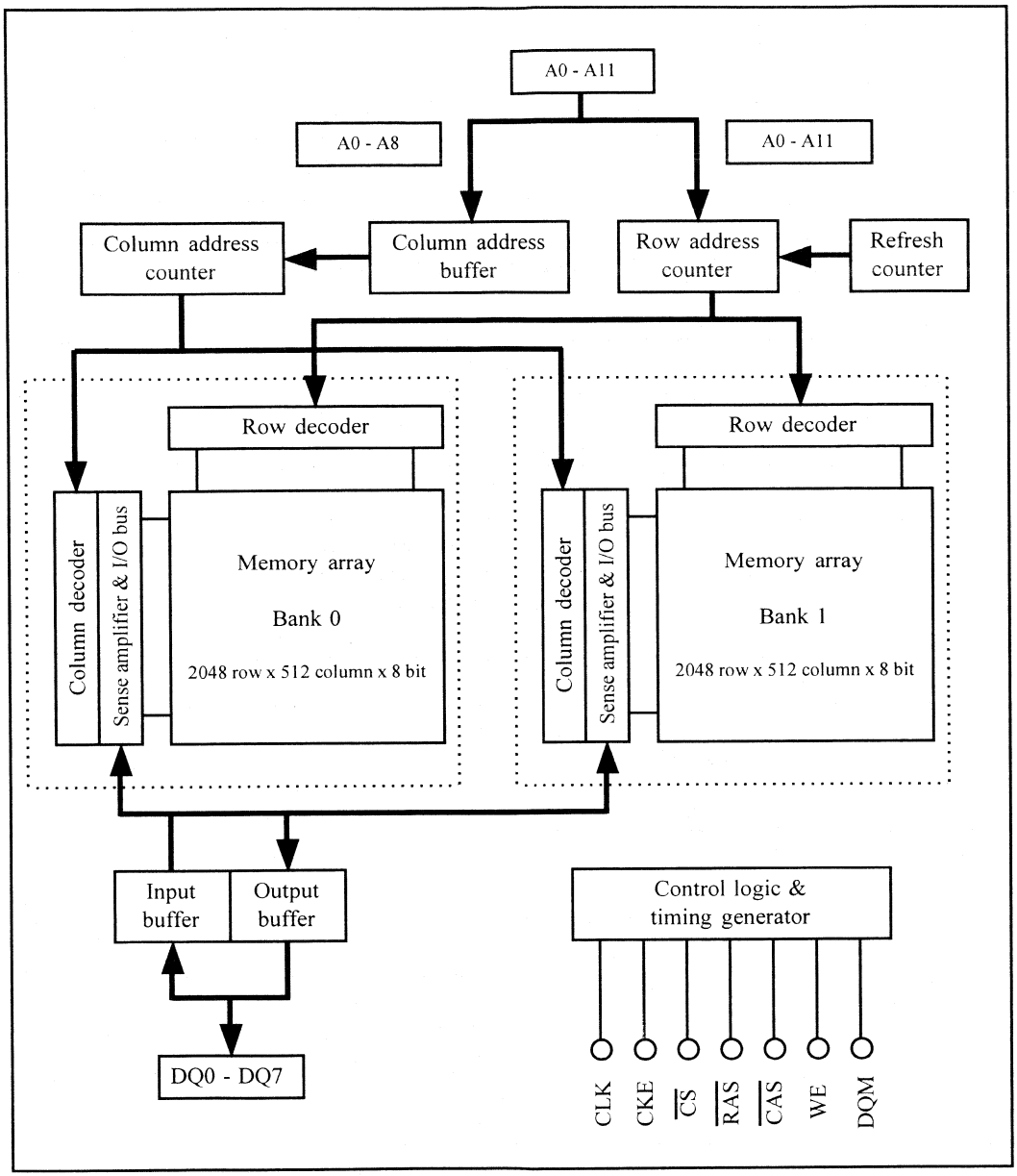


(Top View)

Pin Name

CLK	CLocK input
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ7	Data input / output
DQM	Data input / output Mask
VCCQ	Power for DQ circuit (3.3V)
VSSQ	Power for DQ circuit
VCC	Power for internal circuit (3.3V)
VSS	Ground for internal circuit
NC	No Connection

Block Diagram(GM72V16821DT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V16821DT Series is divided into bank 0 and bank 1. GM72V16821DT Series contain 2048 row x 512 column x 8bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQM (input pins)	DQM controls input/output buffers. • Read operation: If DQM is High, The output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. • Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0~A9
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST]:** This command stops a full-page burst operation (burst length = 512), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY8) and the bank select address (A11). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY8) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY8) and the bank select address (A11).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11(BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self -refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

The GM72V16821DT series can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V16821DT operating instructions.

CKE Truth Table

Current State	Function	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh command REF	H	H	L	L	L	H	X
Idle	Self-refresh entry SELF	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh exit SELFX	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	Other bank READ/READA ILLEGAL on same bank
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Other bank WRIT/WRIT A ILLEGAL on same bank
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	Other bank READ/READA ILLEGAL on same bank
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Other bank WRIT/WRIT A ILLEGAL on same bank
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.

2. An interval of t_{RWL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [READ], [READ A]: Data output by the previous read command continues to be output. After CAS latency, the data output resulting from the next command will start and the currently READA bank precharge is automatically performed. (Attempting to make the currently READA bank READ/READA results in an illegal command.)

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

To [READ], [READ A]: These commands stop a burst write and start a READ/READA cycle and the currently WRITA bank precharge is automatically performed. (Attempting to make the currently WRITA bank READ/READA results in an illegal command.)

To [WRIT], [WRIT A]: These commands stop a burst write, and start a WRIT/WRITA cycle. The currently WRITA bank precharge is automatically performed. (Attempting to make the currently WRITA bank WRIT / WRITA results in an illegal command.)

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-75		-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	100	-	100	-	85	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	2	-	3	-	3	mA	CKE=V_{IL}, t_{CK}=min	5
		I_{CC2}	-	2	-	2	-	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		(100MHz)	-	40	-	40	-	35	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
		(133MHz)	-	55							
Active standby current (Bank Active)		I_{CC3}	-	7	-	7	-	7	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
		(100MHz)	-	45	-	45	-	40	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
		(133MHz)	-	60							
Burst operating current	(CL=1)	I_{CC4}	-	-	-	65	-	55	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)		-	150	-	100	-	85	mA		
	(CL=3)		-	190	-	150	-	125	mA		
Refresh current		I_{CC5}	-	85	-	85	-	70	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	0.4	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0 ≤ Vin ≤ V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0 ≤ Vout ≤ V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)
(GM72V16821DT-10/12)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	2	5	pF	1, 3
Output capacitance (I/O)	C_O	4	7	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)
(GM72V16821DT-75)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2.5	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	2.5	4	pF	1, 3
Output capacitance (I/O)	C_O	4	6.5	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-75		-10		-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9.5	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

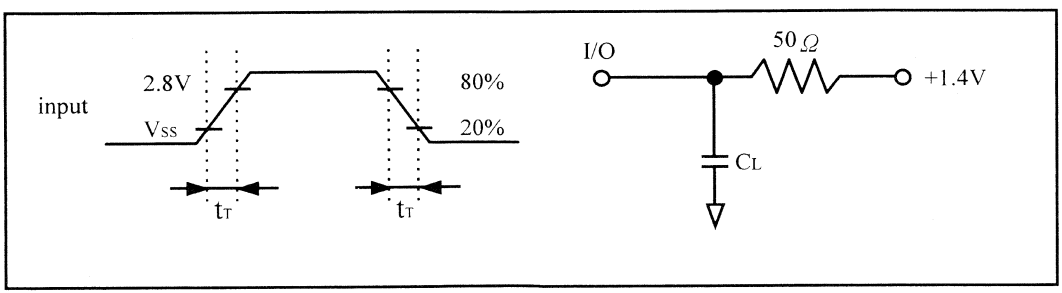
Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.
6. -10 grade products are classified as follows.
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.
   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.
   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

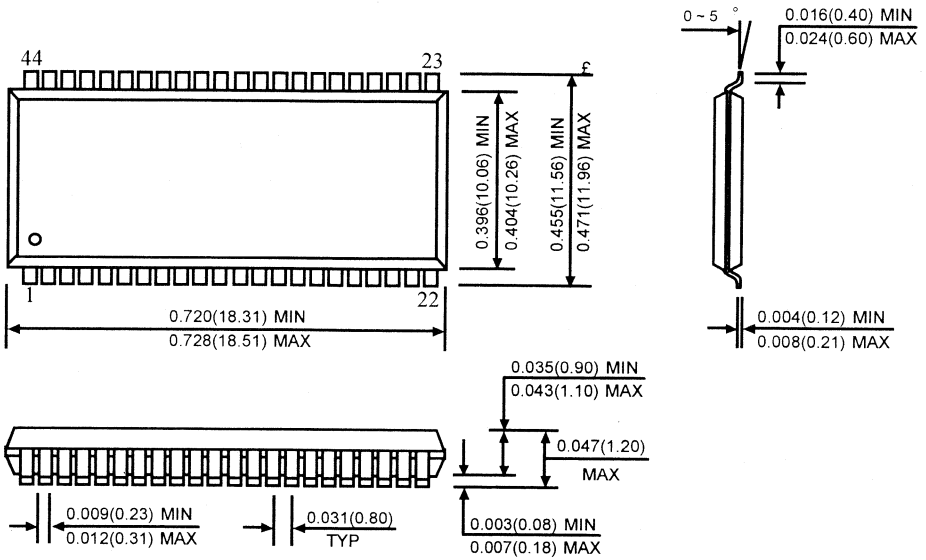
Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-75		-10			-12			Notes
			133	100	100	66	33	83	55	28	
			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

Unit: Inches (mm)

44 TSOP II

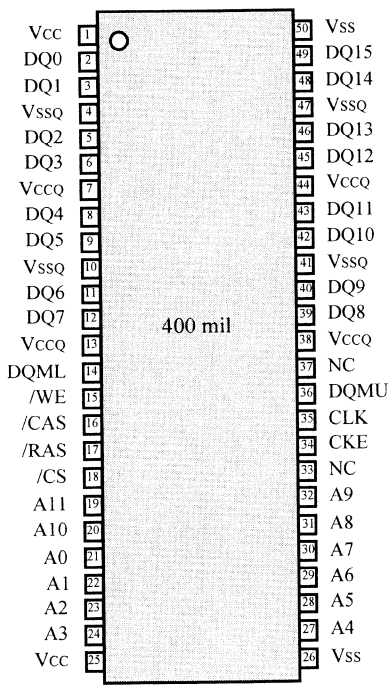


Description

The GM72V161621CT is new generation synchronous dynamic RAM, organized 524,288 words x 16bit x 2bank. This device offers fully synchronous operation referenced to clock rising edge, and mode register allows programmable of burst length, burst type and column access latency. This device is offered in 50pin 400mil plastic TSOP II.

Pin Configuration

50 TSOP II



(Top View)

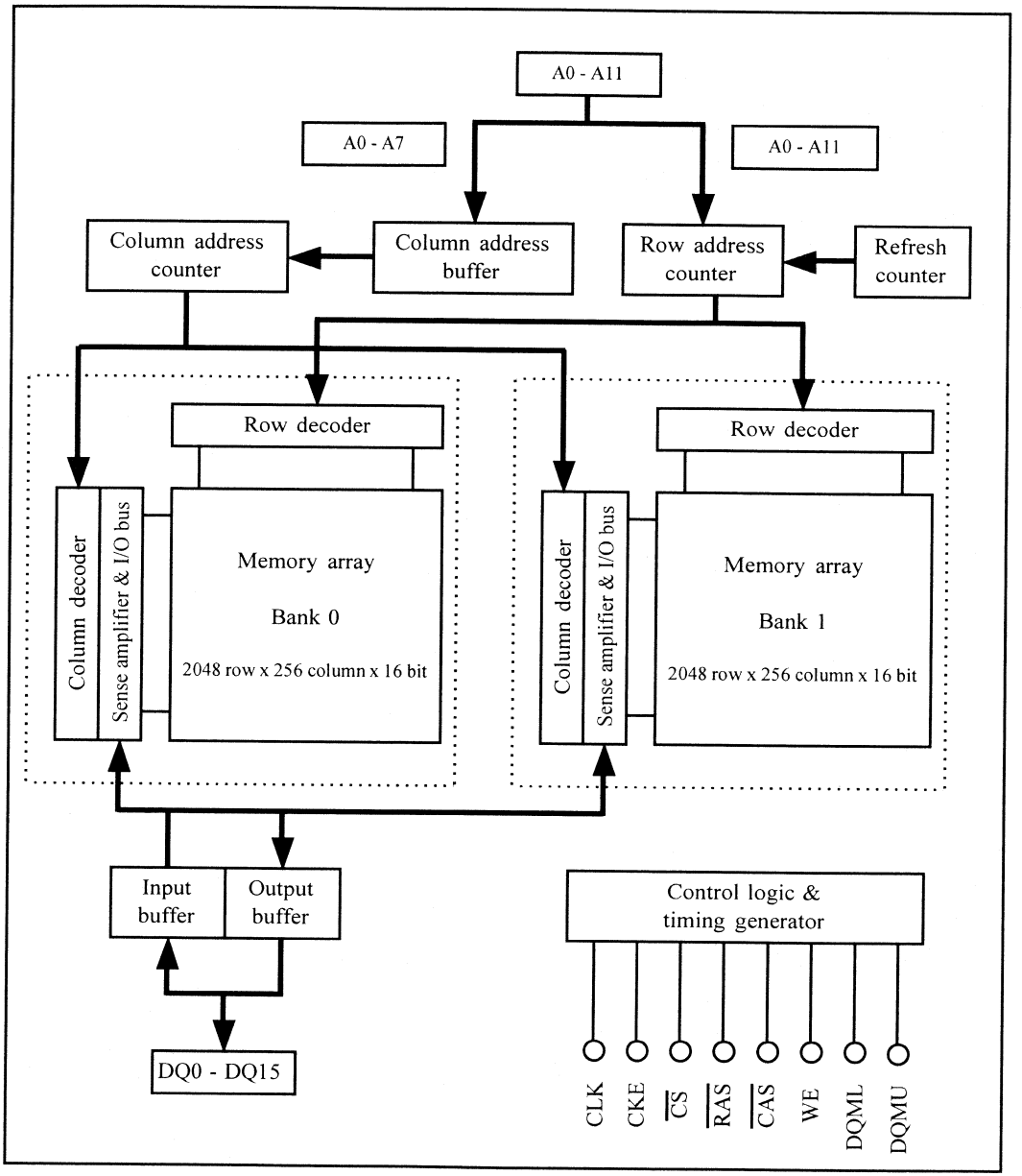
Features

- 524,288 Words x 16 Bit x 2 Bank Organization
- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Single pulsed $\overline{RAS}$
- 2 Bank can operate simultaneously and independently
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence ;
  Sequential (BL = 1, 2, 4, 8, Full page)
  Interleave (BL = 1, 2, 4, 8)
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Byte control by DQMU and DQML
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- 50Pin 400mil TSOP II Package

Pin Name

CLK	CLocK input
$\overline{CKE}$	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
A11 / BS	Address input or Bank Select
DQ0~DQ15	Data input / output
DQMU	Upper byte input / output Mask
DQML	Lower byte input / output Mask
VCCQ	Power for DQ pin(3.3V)
VSSQ	Power for DQ pin
VCC	Power for internal circuit (3.3V)
VSS	Ground for internal circuit
NC	No Connection

Block Diagram(GM72V161621CT Series)



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CLK rising edge. Column address is determined by A0 to A7 level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A11 (BS) is precharged.
A11 (input pin)	A11 is a bank select signal (BS). The memory array of the GM72V161621CT Series is divided into bank 0 and bank 1. GM72V161621CT Series contain 2048 row x 256 column x 16bits. If A11 is Low, bank 0 is selected, and if A11 is High , bank 1 is selected.
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
DQMU, DQML (input pins)	DQMU controls upper byte and DQML controls lower byte input /output buffers. • Read operation: If DQMU/DQML is High, The output buffer becomes High-Z. If the DQMU/DQML is Low, the output buffer becomes Low-Z. • Write operation: If DQMU/DQML is High, the previous data is held (the new data is not written). If DQMU/DQML is Low, the data is written.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A0~A9
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank act.	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST]:** This command stops a full-page burst operation (burst length = full page(256)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7) and the bank select address (A11). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page(256), this command is illegal.

• **Column address strobe and write [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7) and the bank select address (A11) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7) and the bank select address (A11).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A11(BS) and determines the row address (AX0 to AX10). When A11 is Low, bank 0 is activated. When A11 is High, bank 1 is activated

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A11. If A11 is Low, bank 0 is selected. If A11 is High, bank 1 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self -refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQMU	DQML
		n-1	n		
Upper byte write enable/output enable	ENBU	H	X	L	X
Lower byte write inhibit/output enable	ENBL	H	X	X	L
Upper byte write enable/output disable	MASKU	H	X	H	X
Lower byte write inhibit/output disable	MASKL	H	X	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
I_{DOD} is needed.

The GM72V161621CT series can mask input/output data by means of DQMU and DQML. DQMU masks the upper byte and DQML makes the lower byte. During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQM control section of the GM72V161621CT operating instructions.

CKE Truth Table

Current State	Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
		n -1	n					
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh REF command	H	H	L	L	L	H	X
Idle	Self-refresh SELF entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh SELFX exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.

2. An interval of t_{DPL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		-15		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	130	-	105	-	85	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	3	-	3	-	3	mA	CKE=V_{IL}, t_{CK}=min	5
			-	2	-	2	-	2	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	50	-	41	-	33	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
Active standby current (Bank Active)		I_{CC3}	-	7	-	7	-	7	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
			-	51	-	43	-	34	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
Burst operating current	(CL=1)	I_{CC4}	-	65	-	55	-	45	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)	I_{CC4}	-	100	-	85	-	65	mA		
	(CL=3)	I_{CC4}	-	150	-	125	-	100	mA		
Refresh current		I_{CC5}	-	85	-	70	-	60	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0 ≤ Vin ≤ V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0 ≤ Vout ≤ V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	2	5	pF	1, 3
Input capacitance (Signals)	C_{I2}	2	5	pF	1, 3
Output capacitance (I/O)	C_O	4	7	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-10		-12		-15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	45	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-	22.5	-		
	(CL=3)	t_{CK}	10	-	12	-	15	-		
CLK high pulse width		t_{CKH}	3	-	4	-	5	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	5	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	-	36	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12	-	17		
	(CL=3)	t_{AC}	-	7.5	-	9	-	12		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	13	-	15	-	17	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9	-	11		
Data-in setup time		t_{DS}	2	-	3	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	3	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	3	-	3	-	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		- 15		Unit	Notes
		Min	Max	Min	Max	Min	Max		
CKE hold time	t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	100	-	135	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	70	120000	90	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	30	-	45	-	ns	1
Precharge to active command period	t_{RP}	30	-	30	-	45	-	ns	1
Write recovery or data in to Precharge lead time	t_{DPL}	15	-	15	-	22.5	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	20	-	30	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

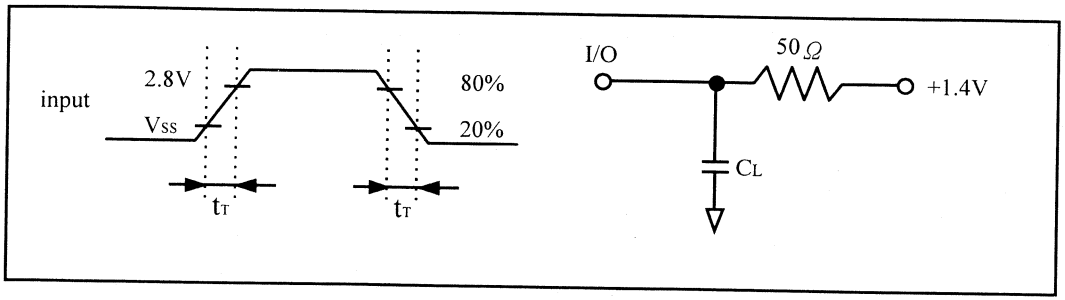
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-10			-12			-15			Notes
			100	66	33	83	55	28	66	44	22	
			10	15	30	12	18	36	15	22.5	45	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	6	4	2	1
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	3	2	1	1
Write recovery or data in to Precharge command(same bank)		t_{DPL}	2	1	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	5	3	2	= [t_{DPL} +t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

(Continued)

Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-10			-12			-15			Notes
			100	66	33	83	55	28	66	44	22	
			10	15	30	12	18	36	15	22.5	45	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	0	

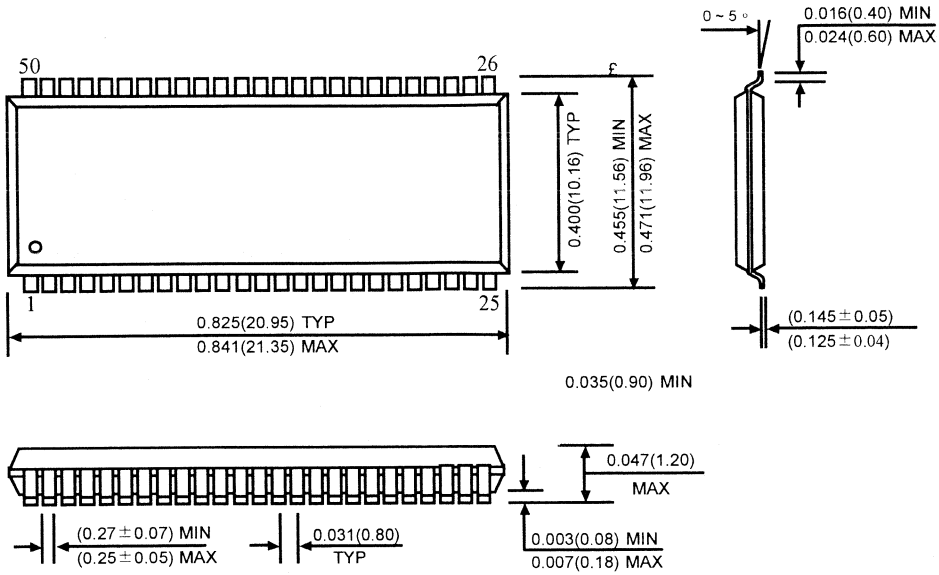
Notes : 1. t_{RCD} to t_{RRD} are recommended value.

2. When self refresh exit is executed, CKE should be kept "H" longer than I_{SREX} from exit cycle.

Package Dimensions

Unit: Inches (mm)

50 TSOP II



LG Semicon Co.,Ltd.

GM72V66441CT -7/8/10

4,194,304 WORD x 4 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

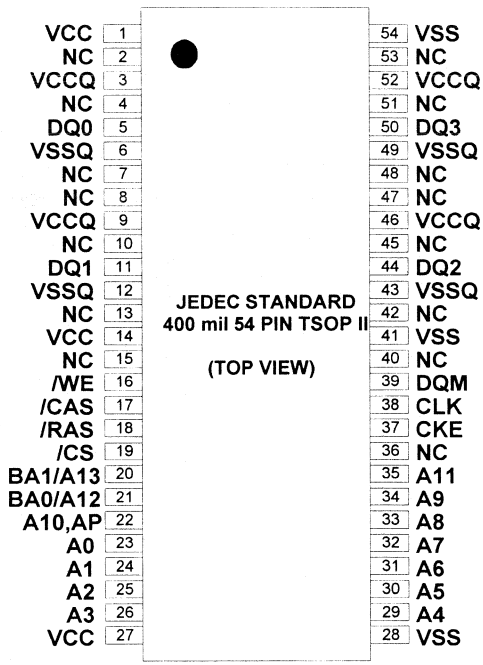
The GM72V66441CT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logics including input and output circuits operating synchronously by refering to the positive edge of the externally provided clock.

The GM72V66441CT provides four banks of 4,194,304 word by 4 bit to realize high bandwidth with the clock frequency up to 125 Mhz.

Features

- 3.3V single power supply
- LVTTL interface
- Max clock frequncy for $\overline{CAS}$ latency of 3
  100/125 MHz
- 4,096 refresh cycle per 64 ms
- Two kind of refresh operation
  Auto refresh/ Self refresh
- Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
- Programmable $\overline{CAS}$ latency : 2/3
- 4 Banks can operate independently or simultaneously
- Burst read/burst write or burst read/single write operation capability
- Input and output masking by DQM input
- One clock of back to back read or write command interval
- Synchronous power down and clock suspend capablity with one clock latency for both entry and exit
- JEDEC Standard 54Pin 400mil TSOP II Package

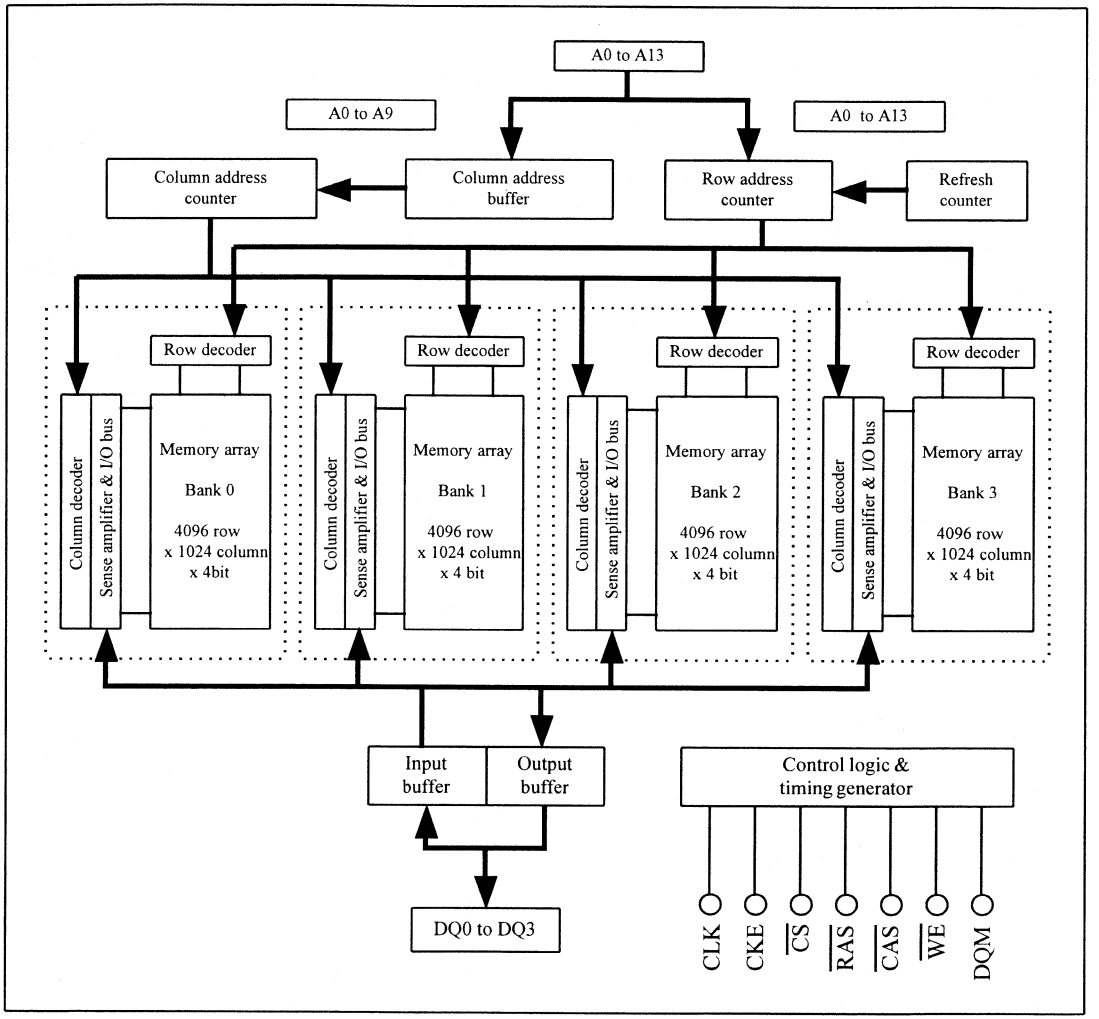
Pin Configuration



Pin Name

CLK	CLocK
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A12~ BA1/A13	Bank select
DQ0~DQ3	Data input / Data ouput
DQM	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Groud for internal circuit
NC	No Connection

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) is determined by A0 to A7, A8 or A9 (A7; GM72V661641CT, A8;GM72V66841CT, A9; GM72V66441CT) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.
A12/A13 (input pin)	A12/A13 are bank select signal (BS). The memory array of the GM72V661641CT, the GM72V66841CT, and the GM72V66441CT is divided into bank 0, bank 1, bank2 and bank 3. GM72V661641CT contain 4096-row x 256-column x 16-bits. GM72V66841CT contain 4096-row x 512-column x 8-bits. GM72V66441CT contain 4096-row x 1024-column x 4-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.
DQM, DQMU/DQML (input pins)	DQM, DQMU/DQML controls input/output buffers. • Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. • Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.

Pin Description(Continued)

Pin Name	DESCRIPTION
DQ0 ~ DQ3 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A12~ A13	A10	A0~ A11
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST] :** This command stops a full-page burst operation (burst length = full-page(256 ; GM72V661641CT, 512 ; GM72V66841CT, 1024 ; GM72V66441CT)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7 ; GM72V661641CT , AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A12/A13(BS) and determines the row address (AX0 to AX11). If A12 is Low and if A13 is Low, bank 0 is activated. If A12 is High and A13 is Low, bank 1 is activated. If A12 is Low and A13 is High, bank 2 is activated. If A12 is High and A13 is High, bank 3 is activated.

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A12/A13. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
Write : I_{DID} is needed.
Read : I_{DOD} is needed.

The GM72V66441CT can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V66441CT operating instructions.

CKE Truth Table

Current State	Function	CKE n -1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh (REF) command	H	H	L	L	L	H	X
Idle	Self-refresh (SELF) entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh (SELFX) exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.
4. BA:Bank Address, RA:Row Address, CA:Column Address

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	55	-	60	-	50	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	75	-	80	-	70	mA		
Standby current in power down		I_{CC2P}	-	3	-	3	-	3	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	2	-	2	-	2	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	20	-	20	-	20	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	9	-	9	-	9	mA	CKE = V_{IH}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	6	-	6	-	6	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	5	-	5	-	5	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	30	-	30	-	30	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	20	-	20	-	20	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	70	-	90	-	70	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	110	-	145	-	110	mA		
Refresh current	(CL= 2)	I_{CC5}	-	80	-	85	-	60	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	130	-	140	-	110	mA		
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 $V_{IL} \leq 0.2V$	7

Parameter	Symbol	-7		-8		-10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq Vcc$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq Vcc$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	-	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	-	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias at the pin under measurement.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, Vss, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

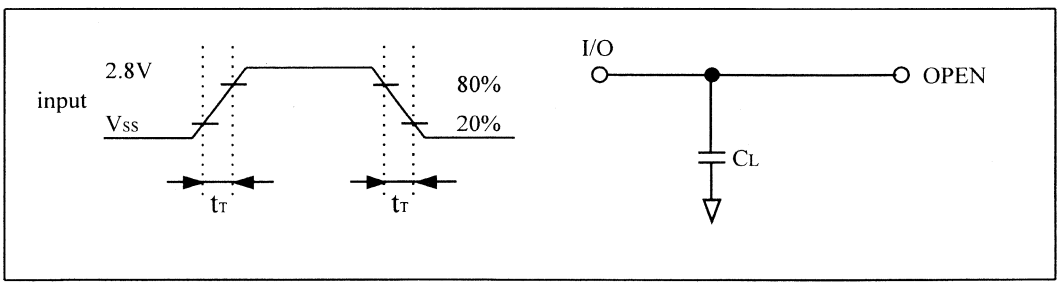
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	1
Active command to active command (same bank)		l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)		l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence	(CL=2)	l_{HZP}	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	l_{EP}	-	-1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

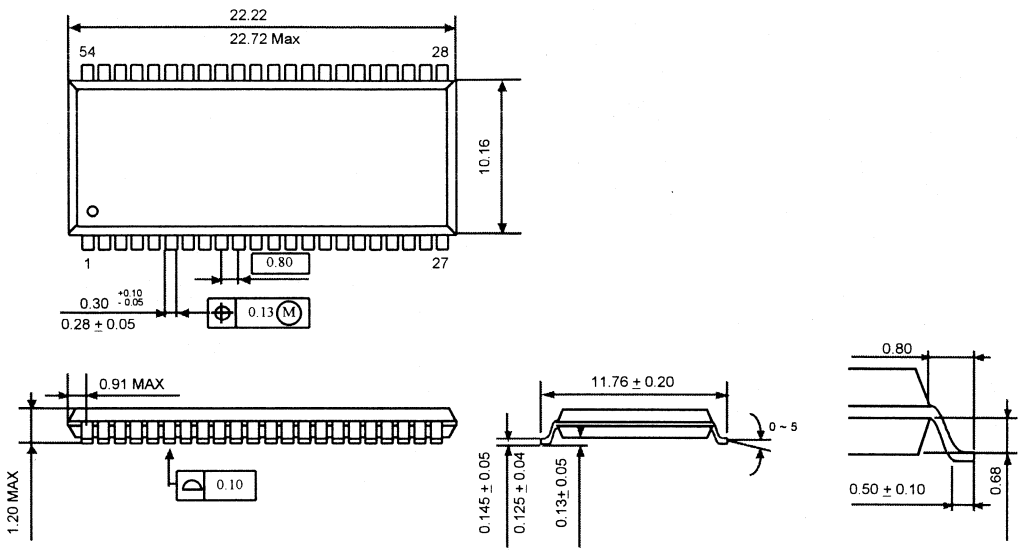
Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

GM72V66441CT Series (TTP-54D)

Preliminary

Unit: (mm)



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-54D
JEDEC Code	-
EIAJ Code	-
Weight(reference value)	0.53g

LG Semicon Co.,Ltd.

GM72V66841CT -7/8/10

2,097,152 WORD x 8 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

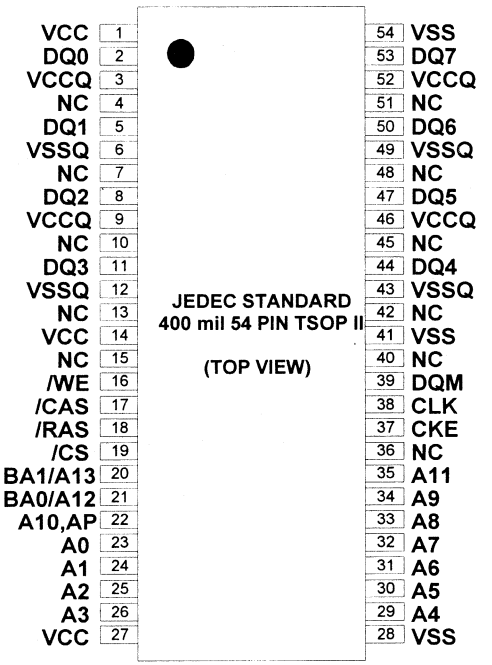
The GM72V66841CT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logics including input and output circuits operating synchronously by refering to the positive edge of the externally provided clock.

The GM72V66841CT provides four banks of 2,097,152 word by 8 bit to realize high bandwidth with the clock frequency up to 125 Mhz.

Features

- 3.3V single power supply
- LVTTL interface
- Max clock frequncy for $\overline{CAS}$ latency of 3
  100/125 MHz
- 4,096 refresh cycle per 64 ms
- Two kind of refresh operation
  Auto refresh/ Self refresh
- Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
- Programmable $\overline{CAS}$ latency : 2/3
- 4 Banks can operate independently or simultaneously
- Burst read/burst write or burst read/single write operation capability
- Input and output masking by DQM input
- One clock of back to back read or write command interval
- Synchronous power down and clock suspend capablity with one clock latency for both entry and exit
- JEDEC Standard 54Pin 400mil TSOP II Package

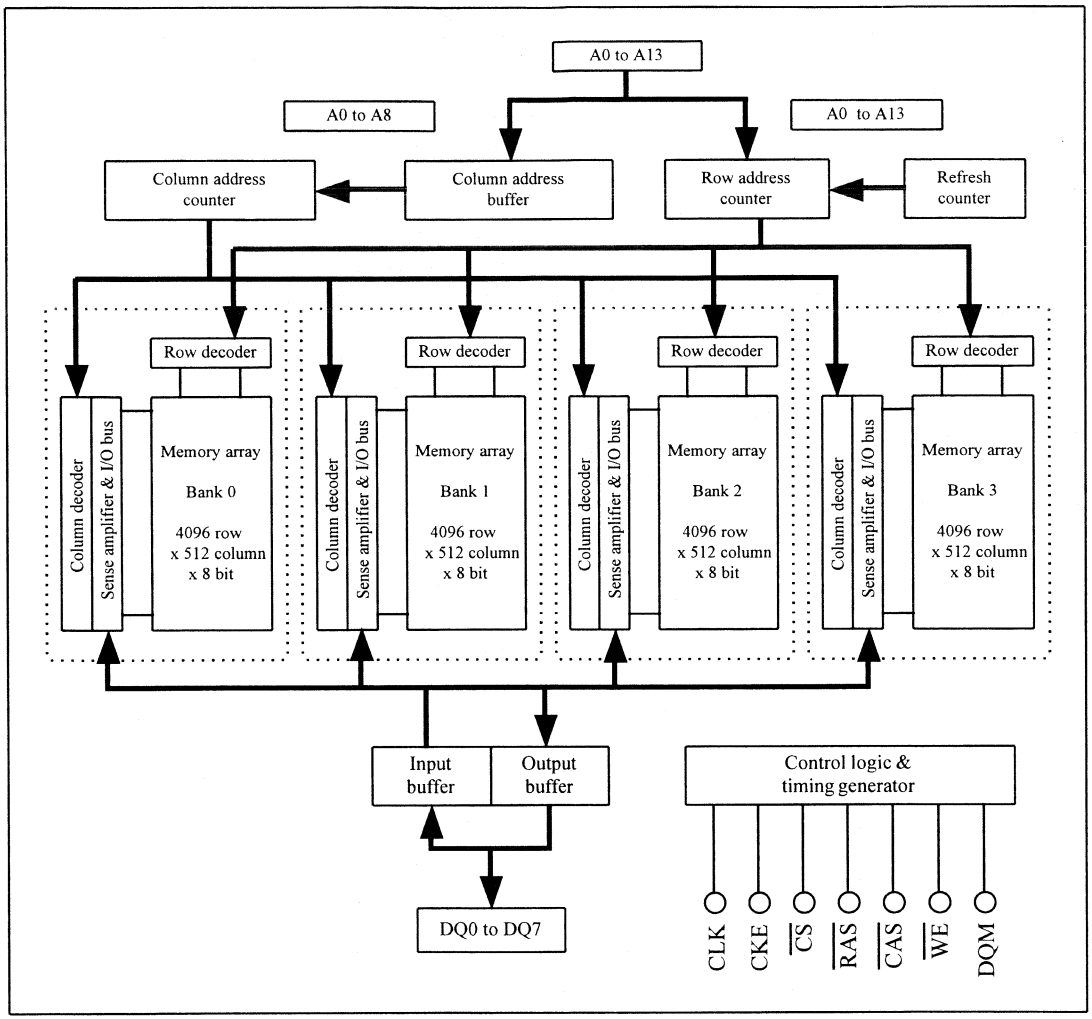
Pin Configuration



Pin Name

CLK	CLocK
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A12	Bank select
~BA1/A13	
DQ0~DQ7	Data input / Data output
DQM	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Groud for internal circuit
NC	No Connection

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) is determined by A0 to A7, A8 or A9 (A7; GM72V661641CT, A8;GM72V66841CT, A9; GM72V66441CT) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.
A12/A13 (input pin)	A12/A13 are bank select signal (BS). The memory array of the GM72V661641CT, the GM72V66841CT, and the GM72V66441CT is divided into bank 0, bank 1, bank2 and bank 3. GM72V661641CT contain 4096-row x 256-column x 16-bits. GM72V66841CT contain 4096-row x 512-column x 8-bits. GM72V66441CT contain 4096-row x 1024-column x 4-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.
DQM, DQMU/DQML (input pins)	DQM, DQMU/DQML controls input/output buffers. • Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. • Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.

Pin Description(Continued)

Pin Name	DESCRIPTION
DQ0 ~ DQ7 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A12~ A13	A10	A0~ A11
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST] :** This command stops a full-page burst operation (burst length = full-page(256 ; GM72V661641CT, 512 ; GM72V66841CT, 1024 ; GM72V66441CT)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7 ; GM72V661641CT , AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A12/A13(BS) and determines the row address (AX0 to AX11). If A12 is Low and if A13 is Low, bank 0 is activated. If A12 is High and A13 is Low, bank 1 is activated. If A12 is Low and A13 is High, bank 2 is activated. If A12 is High and A13 is High, bank 3 is activated.

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A12/A13. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQM
		n-1	n	
Write enable/output enable	ENB	H	X	L
Write inhibit/output disable	MASK	H	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
Write : I_{DID} is needed.
Read : I_{DOD} is needed.

The GM72V66841CT can mask input/output data by means of DQM.
During reading, the output buffer is set to Low-Z by setting DQM to Low, enabling data output. On the other hand, when DQM is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQM to Low. When DQM is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQM. For details, refer to the DQM control section of the GM72V66841CT operating instructions.

CKE Truth Table

Current State	Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
		n -1	n					
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh (REF) command	H	H	L	L	L	H	X
Idle	Self-refresh (SELF) entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh (SELFX) exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.
4. BA:Bank Address, RA:Row Address, CA:Column Address

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, V_{SS}, V_{SSQ}= 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	60	-	65	-	50	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	80	-	85	-	70	mA		
Standby current in power down		I_{CC2P}	-	3	-	3	-	3	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	2	-	2	-	2	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	20	-	20	-	20	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	9	-	9	-	9	mA	CKE = V_{IH}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	6	-	6	-	6	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	5	-	5	-	5	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	30	-	30	-	30	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	20	-	20	-	20	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	70	-	95	-	70	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	120	-	155	-	120	mA		
Refresh current	(CL= 2)	I_{CC5}	-	80	-	85	-	60	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	130	-	140	-	110	mA		
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	$V_{IH} \geq V_{CC}$ - 0.2 $V_{IL} \leq$ 0.2V	7

Parameter	Symbol	- 7		- 8		- 10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq Vcc$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq Vcc$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	-	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	-	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias at the pin under measurement.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

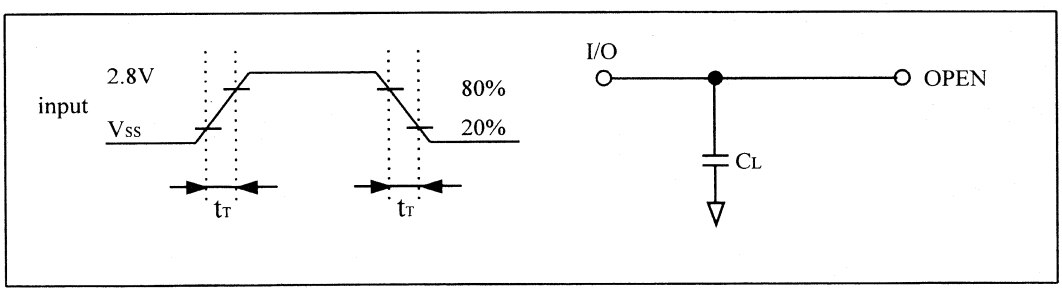
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	1
Active command to active command (same bank)		l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)		l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence	(CL=2)	l_{HZP}	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	l_{EP}	-	- 1	-	- 1	-	- 1	
	(CL=3)	l_{EP}	-2	- 2	-2	- 2	-2	- 2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

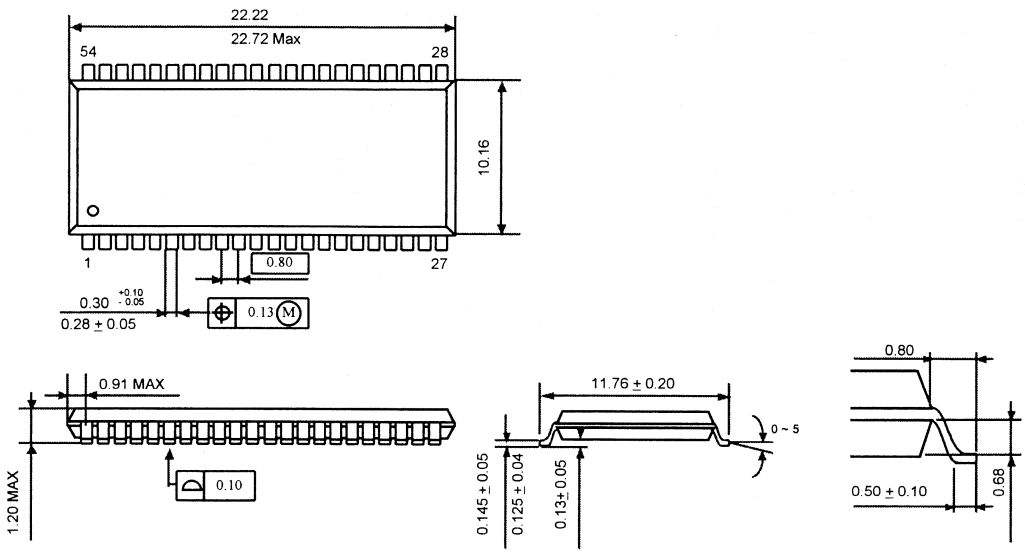
Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

GM72V66841CT Series (TTP-54D)

Preliminary

Unit: (mm)



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-54D
JEDEC Code	-
EIAJ Code	-
Weight(reference value)	0.53g

LG Semicon Co.,Ltd.

GM72V661641CT -7/8/10

1,048,576 WORD x 16 BIT x 4 BANK
SYNCHRONOUS DYNAMIC RAM

Description

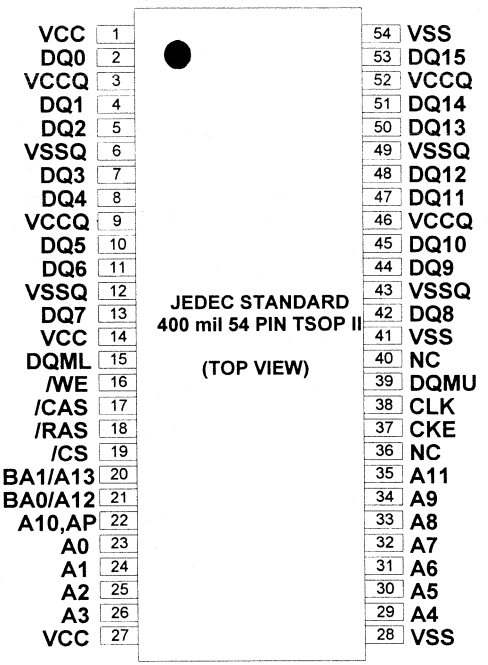
The GM72V661641CT is a synchronous dynamic random access memory comprised of 67,108,864 memory cells and logics including input and output circuits operating synchronously by refering to the positive edge of the externally provided clock.

The GM72V661641CT provides four banks of 1,048,576 word by 16 bit to realize high bandwidth with the clock frequency up to 125 Mhz.

Features

- 3.3V single power supply
- LVTTL interface
- Max clock frequncy for $\overline{CAS}$ latency of 3
  100/125 MHz
- 4,096 refresh cycle per 64 ms
- Two kind of refresh operation
  Auto refresh/ Self refresh
- Programmable burst access capability ;
  - Sequence:Sequential / Interleave
  - Length :1/2/4/8/FP
- Programmable $\overline{CAS}$ latency : 2/3
- 4 Banks can operate independently or simultaneously
- Burst read/burst write or burst read/single write operation capability
- Byte wide input and output control by DQML and DQMU inputs
- One clock of back to back read or write command interval
- Synchronous power down and clock suspend capablity with one clock latency for both entry and exit
- JEDEC Standard 54Pin 400mil TSOP II Package

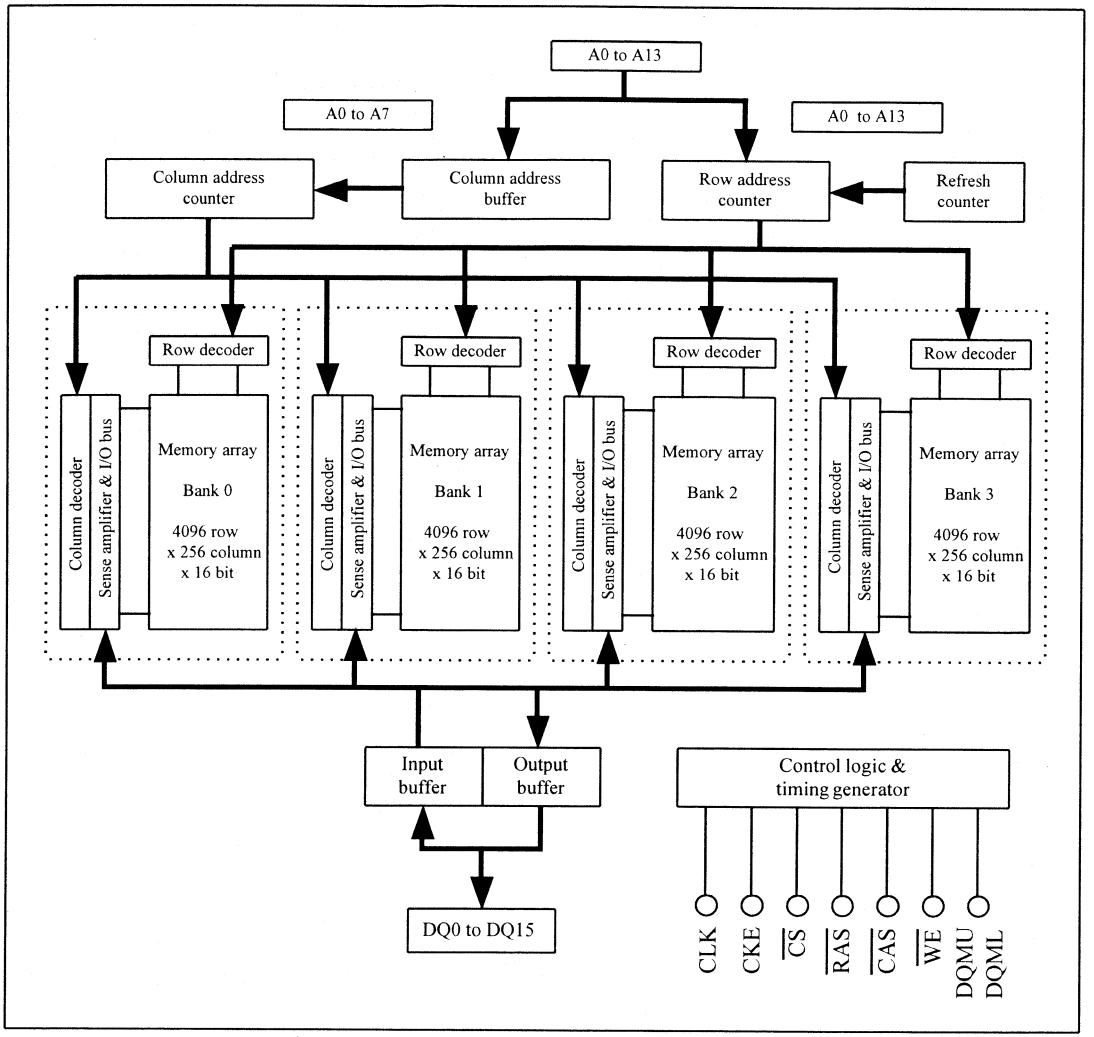
Pin Configuration



Pin Name

CLK	CLocK
CKE	ClocK Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A9,A11	Address input
A10 / AP	Address input or Auto Precharge
BA0/A12	Bank select
~BA1/A13	
DQ0~DQ15	Data input / Data output
DQMU/DQML	Data input / output Mask
VCCQ	Vcc for DQ
VSSQ	Vss for DQ
VCC	Power for internal circuit
VSS	Groud for internal circuit
NC	No Connection

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CLK (input pin)	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE (input pin)	This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{CS}$ (input pin)	When $\overline{CS}$ is Low, the command input cycle becomes valid. When $\overline{CS}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CLK rising edge. Column address(AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) is determined by A0 to A7, A8 or A9 (A7; GM72V661641CT, A8;GM72V66841CT, A9; GM72V66441CT) level at the read or write command cycle CLK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BS) is precharged.
A12/A13 (input pin)	A12/A13 are bank select signal (BS). The memory array of the GM72V661641CT, the GM72V66841CT, and the GM72V66441CT is divided into bank 0, bank 1, bank2 and bank 3. GM72V661641CT contain 4096-row x 256-column x 16-bits. GM72V66841CT contain 4096-row x 512-column x 8-bits. GM72V66441CT contain 4096-row x 1024-column x 4-bits. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.
DQM, DQMU/DQML (input pins)	DQM, DQMU/DQML controls input/output buffers. • Read operation: If DQM, DQMU/DQML is High, The output buffer becomes High-Z. If the DQM, DQMU/DQML is Low, the output buffer becomes Low-Z. • Write operation: If DQM, DQMU/DQML is High, the previous data is held (the new data is not written). If DQM, DQMU/DQML is Low, the data is written.

Pin Description(Continued)

Pin Name	DESCRIPTION
DQ0 ~ DQ15 (I/O pins)	Data is input and ouput from these pins. These pins are the same as those of a conventional DRAM.
V_{CC} and V_{CCQ} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit and V_{CCQ} is for the output buffer.)
V_{SS} and V_{SSQ} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit and V_{SSQ} is for the output buffer.)
NC	No Connection pins.

Command Operation

Command Truth Table

The synchronous DRAM recognizes the following commands specified by the $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and address pins.

Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A12~A13	A10	A0~A11
		n-1	n							
Ignore command	DESL	H	X	H	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop in full page	BST	H	X	L	H	H	L	X	X	X
Column address and read command	READ	H	X	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	X	L	H	L	H	V	H	V
Column address and write command	WRIT	H	X	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	X	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Refresh	REF/SELF	H	V	L	L	L	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	V	V	V

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}, V: Valid address input

• **Ignore command [DESL]:** When this command is set ($\overline{CS}$ is High), the synchronous DRAM ignores command input at the clock. However, the internal status is held.

• **No operation [NOP]:** This command is not an execution command. However, the internal operations continue.

• **Burst stop in full page [BST] :** This command stops a full-page burst operation (burst length = full-page(256 ; GM72V661641CT, 512 ; GM72V66841CT, 1024 ; GM72V66441CT)), and is illegal otherwise. Full page burst continues until this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address, and input/output is performed repeatedly.

• **Column address strobe and read command [READ]:** This command starts a read operation. In addition, the start address of burst read is determined by the column address (AY0 to AY7 ; GM72V661641CT , AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13). After the read operation, the output buffer becomes High-Z.

• **Read with auto-precharge [READ A]:** This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

• **Column address strobe and write command [WRIT]:** This command starts a write operation. When the burst write mode is selected, the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13).

• **Write with auto-precharge [WRIT A]:** This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

• **Row address strobe and bank activate [ACTV]:** This command activates the bank that is selected by A12/A13(BS) and determines the row address (AX0 to AX11). If A12 is Low and if A13 is Low, bank 0 is activated. If A12 is High and A13 is Low, bank 1 is activated. If A12 is Low and A13 is High, bank 2 is activated. If A12 is High and A13 is High, bank 3 is activated.

• **Precharge selected bank [PRE]:** This command starts precharge operation for the bank selected by A12/A13. If A12 is Low and if A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

• **Precharge all banks [PALL]:** This command starts a precharge operation for all banks.

• **Refresh [REF/SELF]:** This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

• **Mode register set [MRS]:** Synchronous DRAM has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A11) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

DQM Truth Table

Function	Symbol	CKE		DQMU	DQML
		n-1	n		
Upper byte write enable/output enable	ENBU	H	X	L	X
Lower byte write enable/output enable	ENBL	H	X	X	L
Upper byte write inhibit/output disable	MASKU	H	X	H	X
Lower byte write inhibit/output disable	MASKL	H	X	X	H

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
Write : I_{DID} is needed.
Read : I_{DOD} is needed.

The GM72V661641CT can mask input/output data by means of DQMU/DQML. DQMU masks the upper byte and DQML masks the lower byte.

During reading, the output buffer is set to Low-Z by setting DQMU/DQML to Low, enabling data output. On the other hand, when DQMU/DQML is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMU/DQML to Low. When DQMU/DQML is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMU/DQML. For details, refer to the DQMU/DQML control section of the GM72V661641CT operating instructions.

CKE Truth Table

Current State	Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
		n -1	n					
Active	Clock suspend mode entry	H	L	H	X	X	X	X
Any	Clock suspend	L	L	X	X	X	X	X
Clock Suspend	Clock suspend mode exit	L	H	X	X	X	X	X
Idle	Auto-refresh (REF) command	H	H	L	L	L	H	X
Idle	Self-refresh (SELF) entry	H	L	L	L	L	H	X
Idle	Power down entry	H	L	L	H	H	H	X
		H	L	H	X	X	X	X
Self refresh	Self refresh (SELFX) exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X
Power down	Power down Exit	L	H	L	H	H	H	X
		L	H	H	X	X	X	X

* Notes : H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.

• **Clock suspend mode entry:** The synchronous DRAM enters clock suspend mode from active mode by setting CKE to Low. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

• **ACTIVE clock suspend:** This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

• **READ suspend and READ A suspend:** The data being output is held (and continues to be output).

• **WRITE suspend and WRIT A suspend:** In this mode, external signals are not accepted. However, the internal state is held.

• **Clock suspend:** During clock suspend mode, keep the CKE to Low.

• **Clock suspend mode exit :** The synchronous DRAM exits from clock suspend mode by setting CKE to High during the clock suspend state.

• **IDLE:** In this state, all banks are not selected, and completed precharge operation.

• **Auto-refresh command[REF]:** When this command is input from the IDLE state, the synchronous DRAM starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the synchronous DRAM. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4,096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

• **Self-refresh entry[SELF]:** When this command is input during the IDLE state, the synchronous DRAM starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

• **Self-refresh exit[SELFX]:** When this command is executed during self-refresh mode, the synchronous DRAM can exit from self-refresh mode. After exiting from self-refresh mode, the synchronous DRAM enters the IDLE state.

• **Power down mode entry:** When this command is executed during the IDLE state, the synchronous DRAM enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

• **Power down exit:** When this command is executed at the power down mode, the synchronous DRAM can exit from power down mode. After exiting from power down mode, the synchronous DRAM enters the IDLE state.

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the synchronous DRAM.

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	H	X	X	X	X	DESL	Enter IDLE after t_{RP}
	L	H	H	H	X	NOP	Enter IDLE after t_{RP}
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	NOP

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Precharge	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set
Row active	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Read	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CAS}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Write	H	X	X	X	X	DESL	Continue burst to end
	L	H	H	H	X	NOP	Continue burst to end
	L	H	H	L	X	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and precharge*2
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	X	X	X	X	DESL	Continue burst to end and precharge
	L	H	H	H	X	NOP	Continue burst to end and precharge
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	Other bank active *3 ILLEGAL on same bank
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Function Truth Table (Continued)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Operation
Refresh (auto-refresh)	H	X	X	X	X	DESL	Enter IDLE after t_{RC}
	L	H	H	H	X	NOP	Enter IDLE after t_{RC}
	L	H	H	L	X	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL
	L	L	H	H	BA, RA	ACTV	ILLEGAL
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL
	L	L	L	H	X	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

* Notes : 1. H: V_{IH}, L: V_{IL}, X: V_{IH} or V_{IL}.
The other combinations are inhibit.
2. An interval of t_{RWL} is required between the final valid data input and the precharge command.
3. If t_{RRD} is not satisfied, this operation is illegal.
4. BA:Bank Address, RA:Row Address, CA:Column Address

From [PRECHARGE]

To [DESL], [NOP] or [BST]: When these commands are executed, the synchronous DRAM enters the IDLE state after t_{RP} has elapsed from the completion of precharge

From [IDLE]

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The synchronous DRAM enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The synchronous DRAM enters the mode register set cycle.

From [ROW ACTIVE]

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the synchronous DRAM to precharge mode. (However, an interval of t_{RAS} is required.)

From [READ]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CAS}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop a burst read, and the synchronous DRAM enters precharge mode.

From [READ with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes other banks bank-active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From [WRITE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the synchronous DRAM then enters precharge mode.

From [WRITE with AUTO-PRECHARGE]

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed, and the synchronous DRAM then enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RC} is required.) Attempting to make the currently active bank active results in an illegal command.

From [REFRESH]

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the synchronous DRAM automatically enters the Idle state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	70	-	75	-	60	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	90	-	95	-	80	mA		
Standby current in power down		I_{CC2P}	-	3	-	3	-	3	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	2	-	2	-	2	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	20	-	20	-	20	mA	CKE,CS = V_{IH}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	9	-	9	-	9	mA	CKE = V_{IH}, t_{CK} = ∞	4
Active standby current in power down		I_{CC3P}	-	6	-	6	-	6	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	5	-	5	-	5	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	30	-	30	-	30	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	20	-	20	-	20	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	120	-	145	-	120	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	170	-	205	-	170	mA		
Refresh current	(CL= 2)	I_{CC5}	-	80	-	85	-	60	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	130	-	140	-	110	mA		
Self refresh current		I_{CC6}	-	2	-	2	-	2	mA	V_{IH} ≥ V_{CC} - 0.2 V_{IL} ≤ 0.2V	7

Parameter	Symbol	- 7		- 8		- 10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V)

Parameter	Symbol	Typ.	Max.	Unit	Notes
Input capacitance (CLK)	C_{I1}	-	4	pF	1, 3, 4
Input capacitance (Signals)	C_{I2}	-	5	pF	1, 3, 4
Output capacitance (DQ)	C_O	-	6.5	pF	1, 2, 3, 4

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQM, DQMU/DQML = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.
4. Measured with 1.4 V bias at the pin under measurement.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

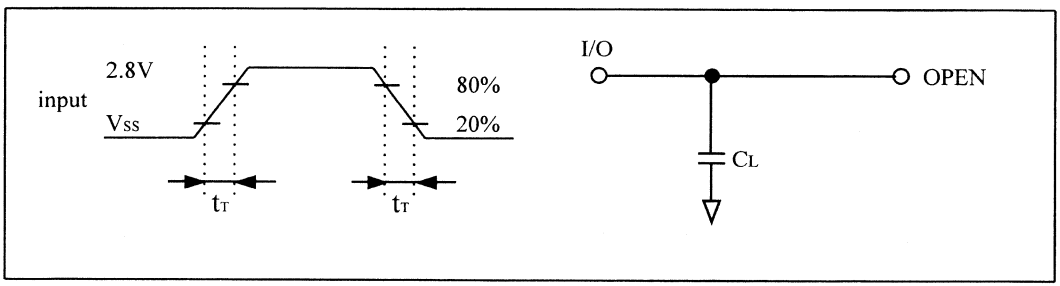
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	- 7		- 8		- 10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	1
Active command to active command (same bank)		l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)		l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence	(CL=2)	l_{HZP}	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	l_{EP}	-	-1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	

Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

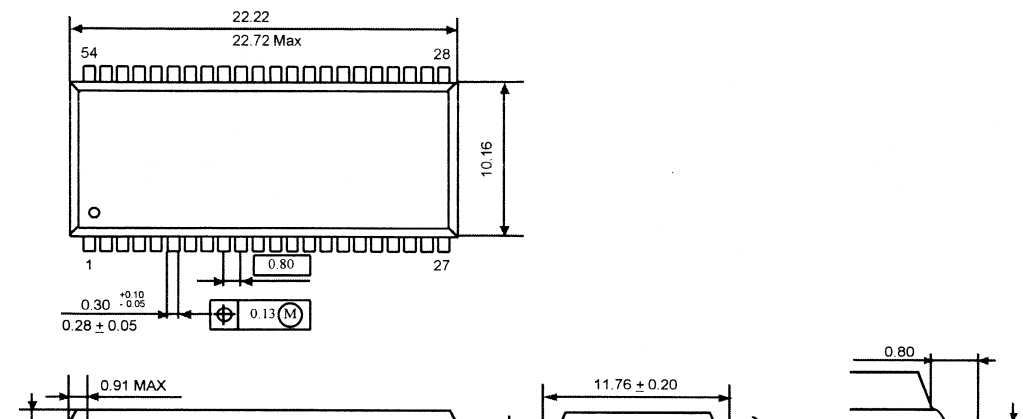
Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimensions

GM72V661641CT Series (TTP-54D)

Preliminary

Unit: (mm)



Hitachi Code	TTP-54D
JEDEC Code	-
EIAJ Code	-
Weight(reference value)	0.53g

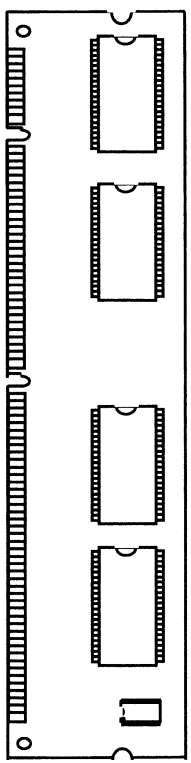
Dimension including the plating thickness
Base material dimension

Description

The GMM2642233CNTG is a 2M x 64bits Synchronous Dynamic RAM MODULE which is assembled 8 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2642233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2642233CNTG provides common data inputs and outputs.

- **GMM2642233CNTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66/83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

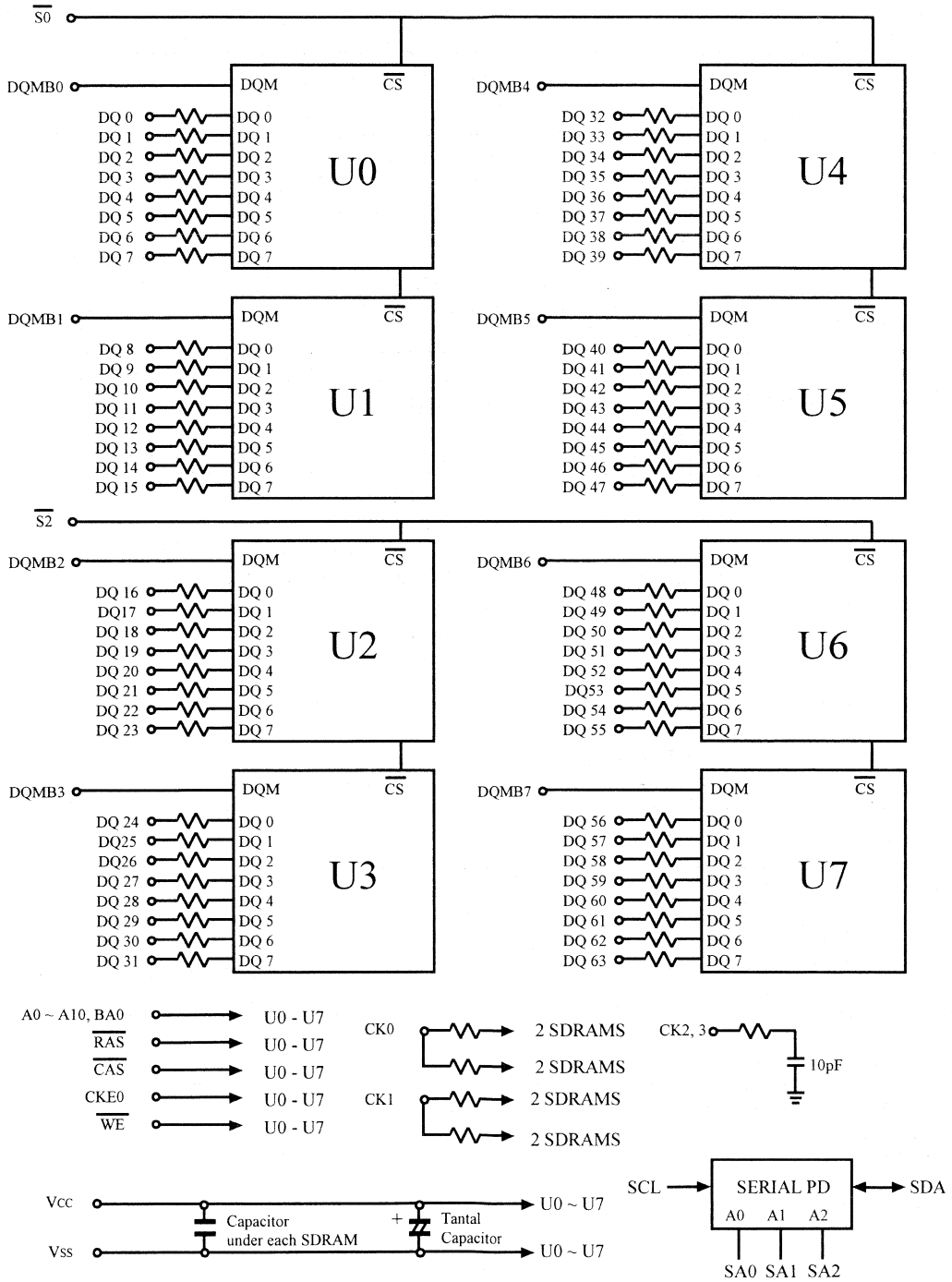
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	*$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	*$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	NC	49	Vcc	77	DQ31	105	NC	133	Vcc	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 2 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS Latency	1, 2 & 3	07h	
19	$\overline{CS}$ Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		1Eh	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2642233CNTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			32h	2
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			4Eh	N
85			54h	T
86			47h	G

Byte No.	Function description	Function support	Hex Value	Note
87			2Dh	-
88			31h	1
89			30h	0
90			4Bh	K
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 w/k
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

• Above data are based on the SPD specification of JEDEC standard and can be changed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	8	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	800	-	680	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	24	-	24	mA	CKE=V_{IL}, t_{CK}=min	5
			-	16	-	16	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	240	-	200	mA	CKE=V_{IL} NOP command t_{CK}=min	3
Active standby current (Bank Active)		I_{CC3}	-	56	-	56	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	280	-	240	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	800	-	680	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1200	-	1000	mA		
Auto Refresh current		I_{CC5}	-	680	-	560	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	16	-	16	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	60	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	55	pF	1, 3
C_{I3}	Input capacitance (CK0, CK1)	-	50	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	30	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	20	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	18	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12		
	(CL=3)	t_{AC}	-	7.5	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	-10		-12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

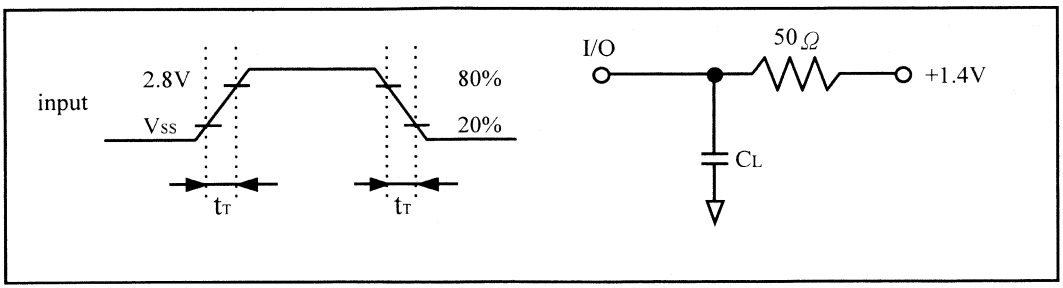
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

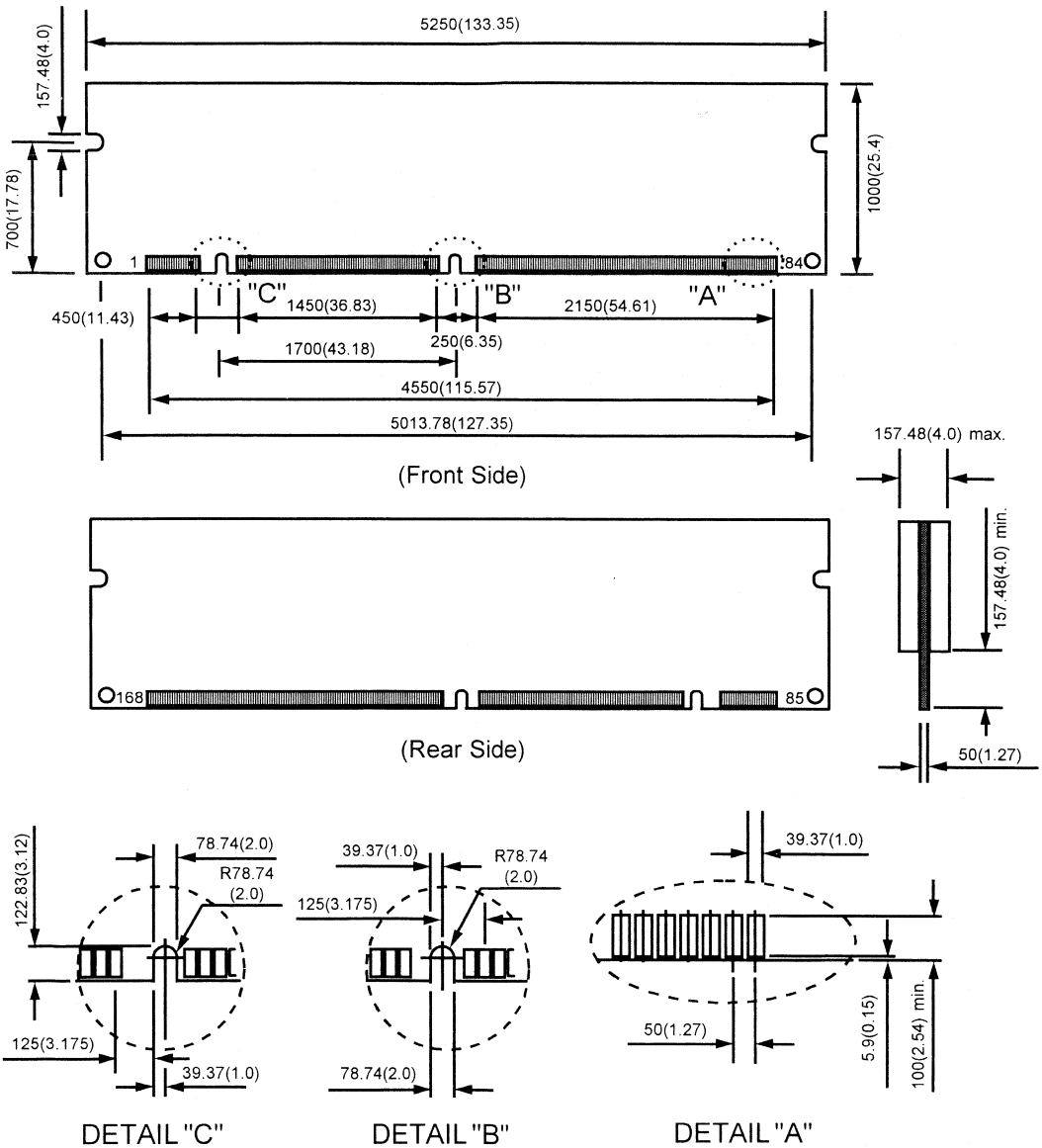
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		ICLE	1	1	1	1	1	1	
Register set to active command		tRSA	1	1	1	1	1	1	
CS to command disable		ICDD	0	0	0	0	0	0	
Power down exit to command input		IPEC	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	IBSR	2	2	2	2	2	2	
	(CL=2)	IBSR	-	1	1	-	1	1	
	(CL=1)	IBSR	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	IBSH	3	3	3	3	3	3	
	(CL=2)	IBSH	-	2	2	-	2	2	
	(CL=1)	IBSH	-	-	1	-	-	1	
Burst stop to write data ignore		IBSW	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM2642233DNTG

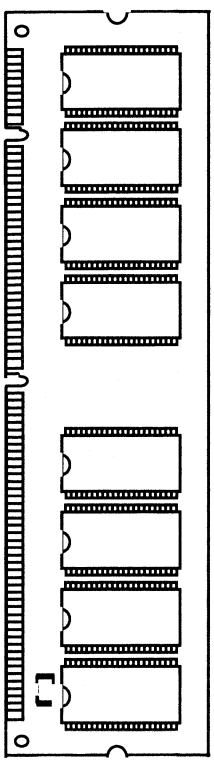
2,097,152 WORDS x64bit
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2642233DNTG is a 2M x 64bits Synchronous Dynamic RAM MODULE which is assembled 8 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2642233DNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2642233DNTG provides common data inputs and outputs.

- **GMM2642233DNTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

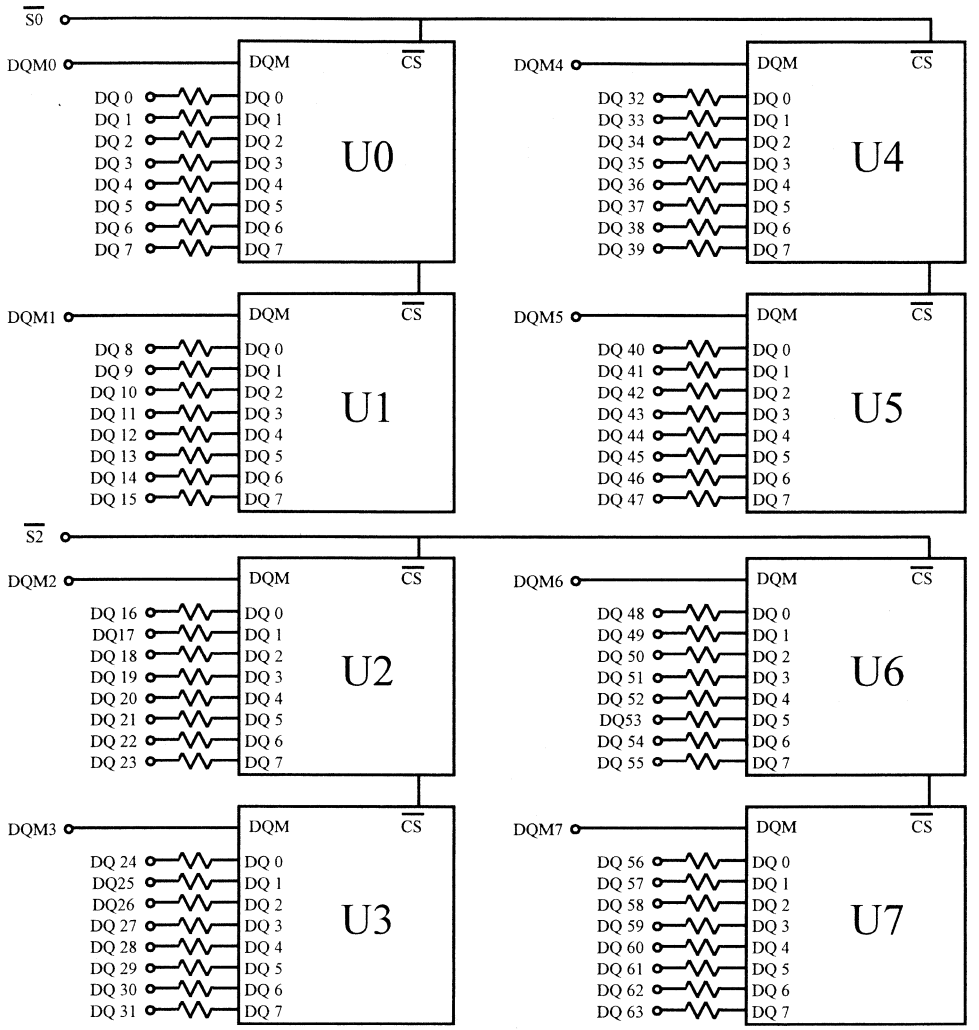
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

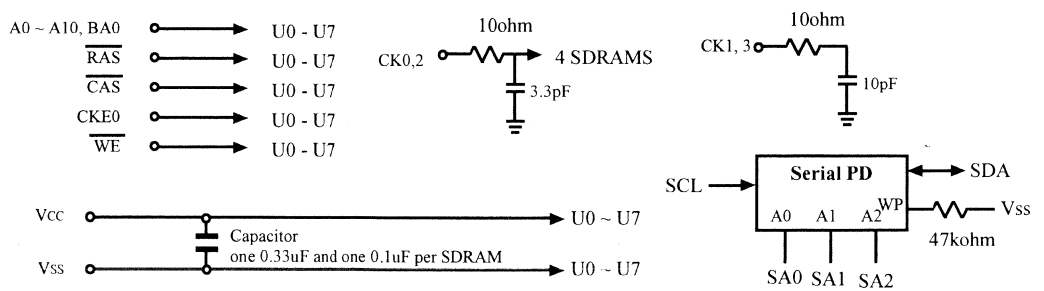
Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram





Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=7.5ns	75h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=6.0ns	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=14ns	0Eh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=48ns	30h	
31	Module Bank Density	16MBytes	04h	
32	Command & address signal input setup time	t_{CS} = 2ns	20h	
33	Command & address signal input hold time	t_{CH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		B4h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2642233DNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			32h	2
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			44h	D
84			4Dh	N
85			54h	T
86			47h	G
87			2Dh	-
88			37h	7
89			4Ah	J
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		AFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter	Symbol	-75		-10		-12		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	-	800	-	800	-	680	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	-	16	-	24	-	24	mA	CKE=V_{IL}, t_{CK}=min	5
	I_{CC2}	-	16	-	16	-	16	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
	(100MHz)	-	320	-	320	-	280	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
	(133MHz)	-	440							
Active standby current (Bank Active)	I_{CC3}	-	56	-	56	-	56	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
	(100MHz)	-	360	-	360	-	360	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
	(133MHz)	-	480							
Burst operating current (CL=1)	I_{CC4}	-	-	-	520	-	440	mA	t_{CK}=min BL = 4	1, 2, 4
Burst operating current (CL=2)		-	1200	-	800	-	680	mA		
Burst operating current (CL=3)		-	1520	-	1200	-	1000	mA		
Refresh current	I_{CC5}	-	680	-	680	-	560	mA	t_{RC}=min	
Self refresh current	I_{CC6}	-	3.2	-	16	-	16	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	0 ≤ Vin ≤ V_{CC}	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	0 ≤ Vout ≤ V_{CC} I/O = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1,2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 75		- 10		- 12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

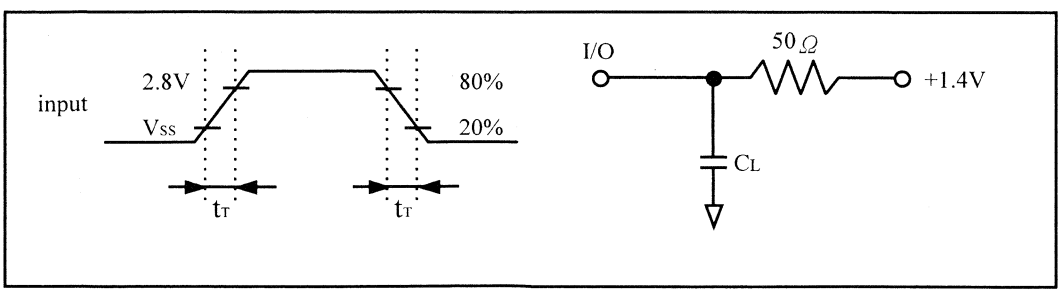
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-75		-10			-12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

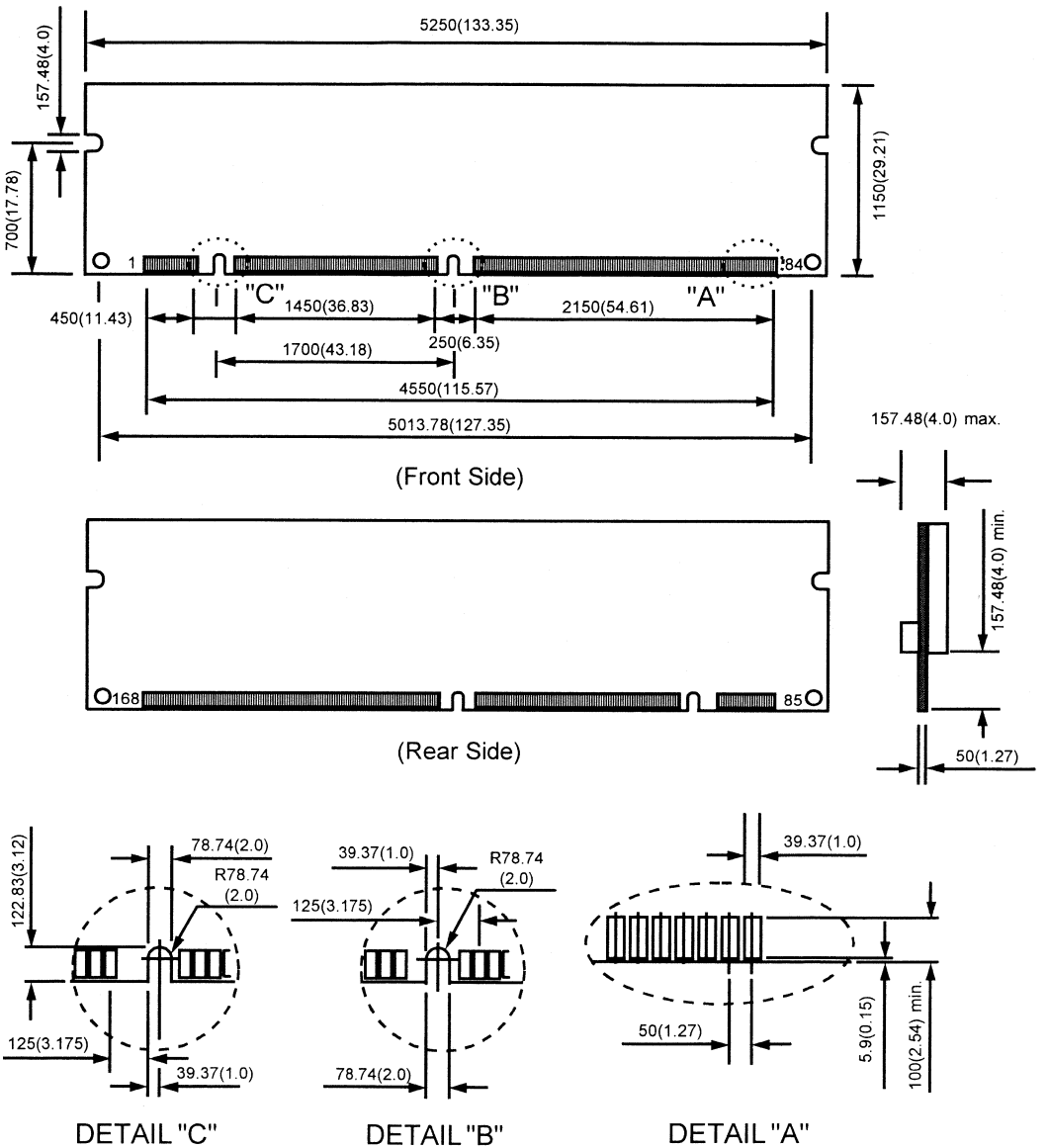
Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM2732233CTG

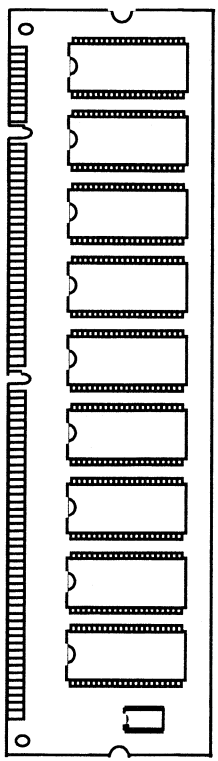
2,097,512 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2732233CTG is a 2M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2732233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2732233CTG provides common data inputs and outputs.

- **GMM2732233CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

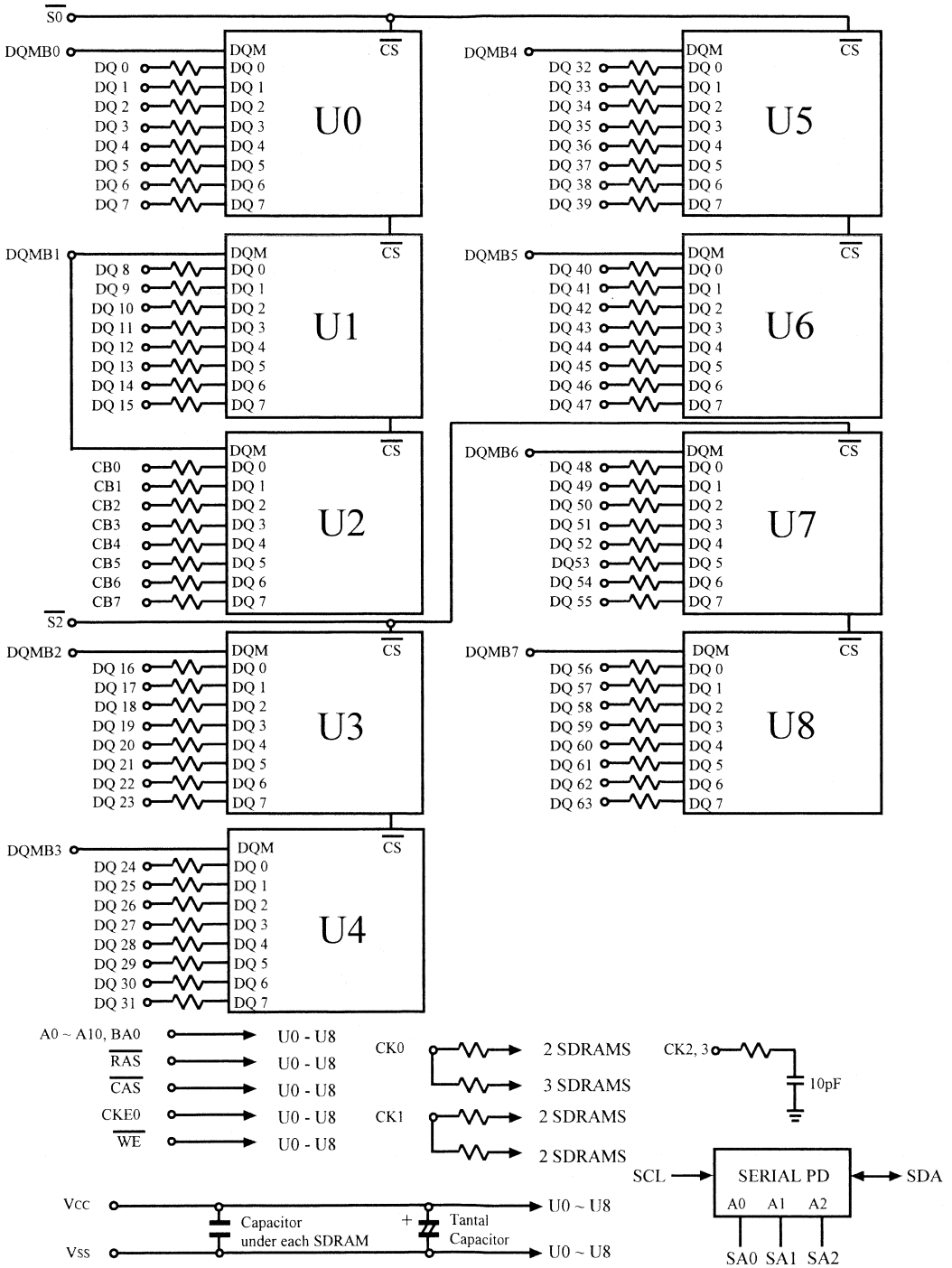
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 2 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		30h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2732233CTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			32h	2
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			54h	T
85			47h	G
86			2Dh	-

Byte No.	Function description	Function support	Hex Value	Note
87			31h	1
88			30h	0
89			4Bh	K
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	9	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	900	-	765	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	27	-	27	mA	CKE=V_{IL}, t_{CK}=min	5
			-	18	-	18	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	270	-	225	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	63	-	63	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	315	-	270	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	900	-	765	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1350	-	1125	mA		
Auto Refresh current		I_{CC5}	-	765	-	630	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	18	-	18	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	Vcc	2.4	Vcc	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	60	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	60	pF	1, 3
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	70	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	35	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	17	pF	1, 3
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	17	pF	1, 2, 3

Note :
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12		
	(CL=3)	t_{AC}	-	7.5	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

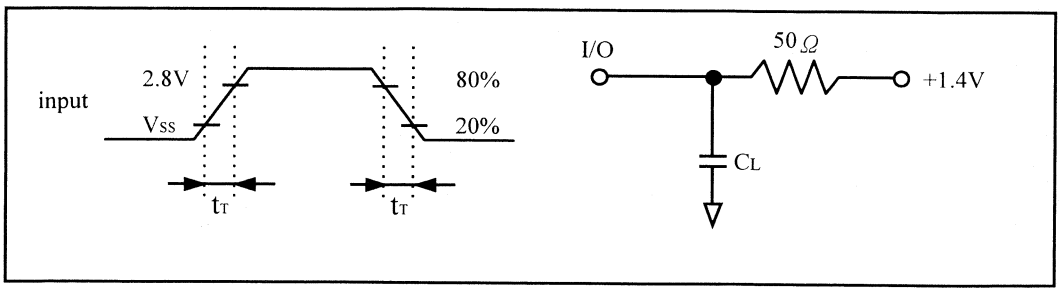
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

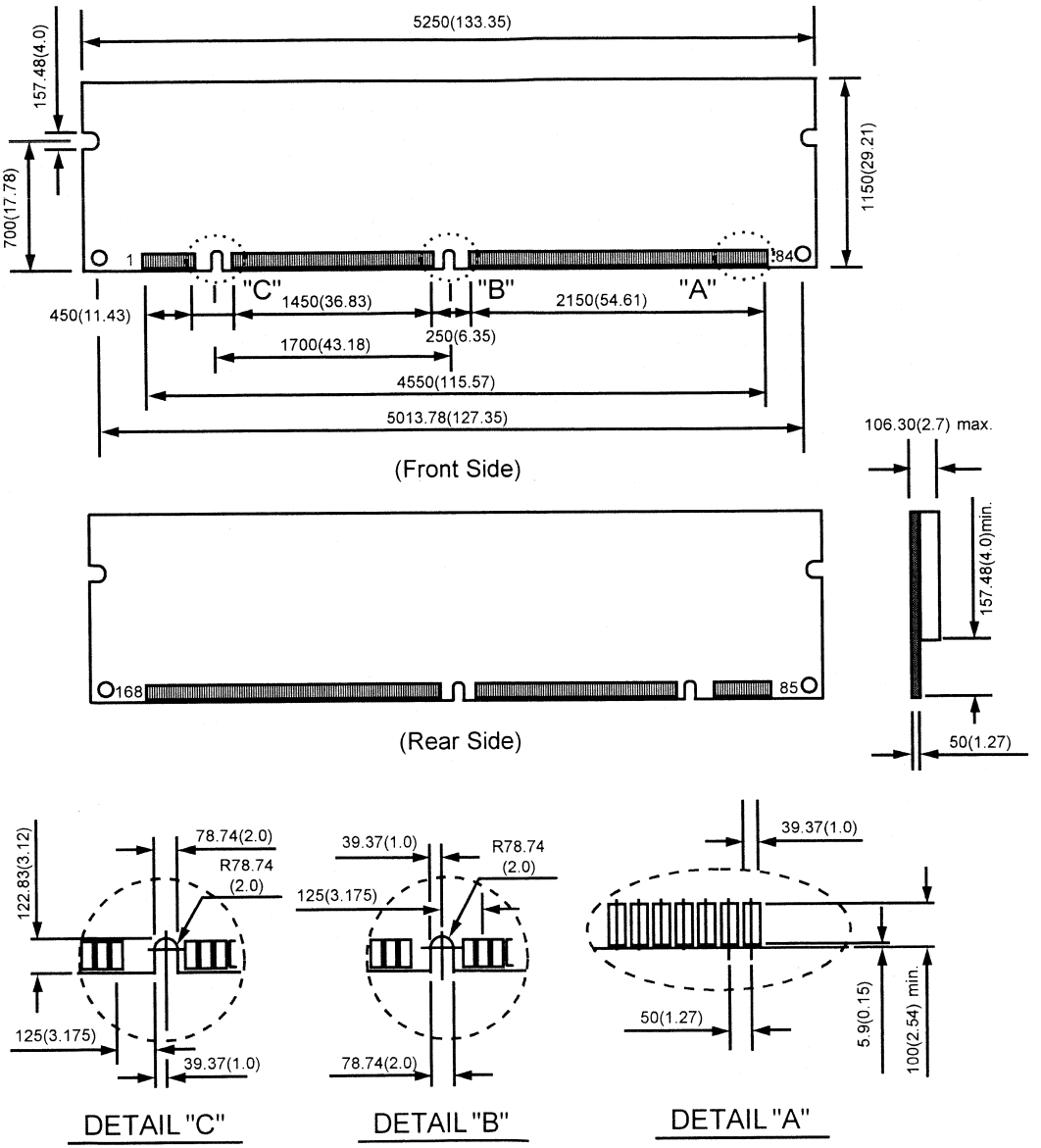
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



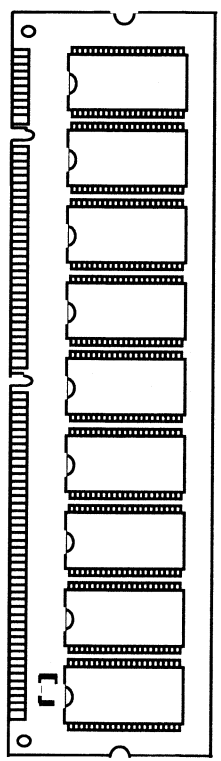
NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

Description

The GMM2732233DTG is a 2M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2732233DTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2732233DTG provides common data inputs and outputs.

- **GMM2732233DTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

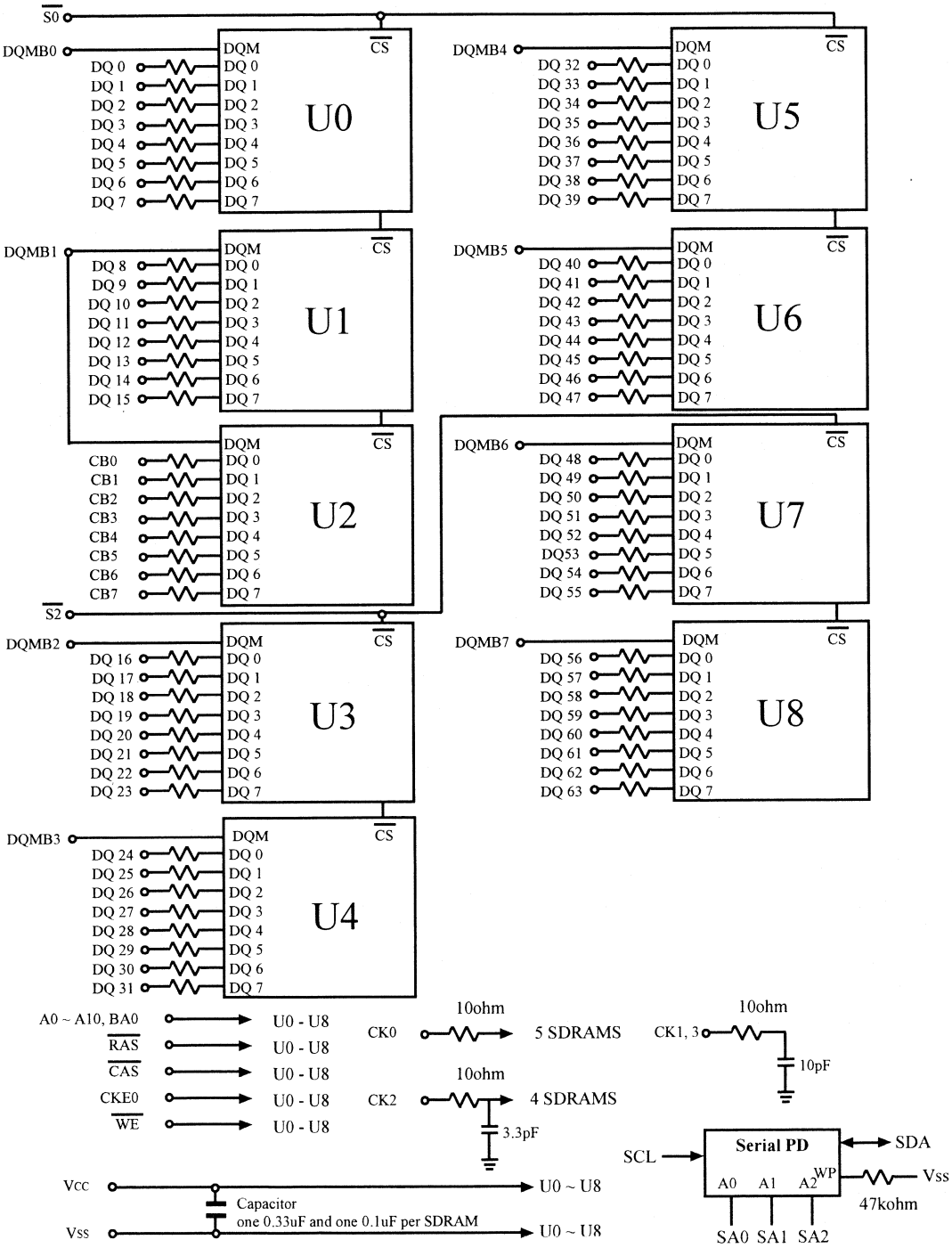
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=7.5ns	75h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=6.0ns	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=14ns	0Eh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=48ns	30h	
31	Module Bank Density	16MBytes	04h	
32	Command & address signal input setup time	t_{CS} = 2ns	20h	
33	Command & address signal input hold time	t_{CH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
36~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		C6h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2732233DTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			32h	2
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			44h	D
84			54h	T
85			47h	G
86			2Dh	-
87			37h	7
88			4Ah	J
89			20h	null
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		AFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter	Symbol	-75		-10		-12		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Operating current	I_{CC1}	-	900	-	900	-	765	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	-	18	-	27	-	27	mA	CKE=V_{IL}, t_{CK}=min	5
	I_{CC2}	-	18	-	18	-	18	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
	(100MHz)	-	360	-	360	-	315	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
	(133MHz)	-	495							
Active standby current (Bank Active)	I_{CC3}	-	63	-	63	-	63	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
	(100MHz)	-	405	-	405	-	360	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
	(133MHz)	-	540							
Burst operating current (CL=1)	I_{CC4}	-	-	-	585	-	495	mA	t_{CK}=min BL = 4	1, 2, 4
Burst operating current (CL=2)		-	1350	-	900	-	765	mA		
Burst operating current (CL=3)		-	1710	-	1350	-	1125	mA		
Refresh current	I_{CC5}	-	765	-	765	-	630	mA	t_{RC}=min	
Self refresh current	I_{CC6}	-	3.6	-	18	-	18	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	0≤Vin≤V_{CC}	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	0≤Vout≤V_{CC} I/O = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB1)	-	TBD	pF	1, 2
C_{I6}	Input capacitance (DQMB0, 2, 3, 4, 5, 6, 7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 75		- 10		- 12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

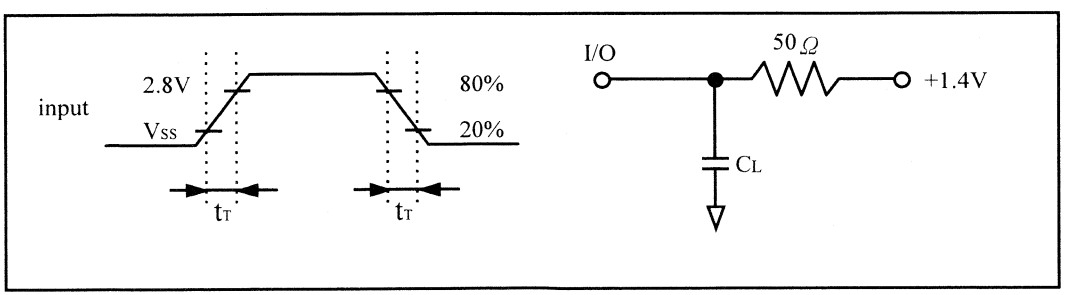
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

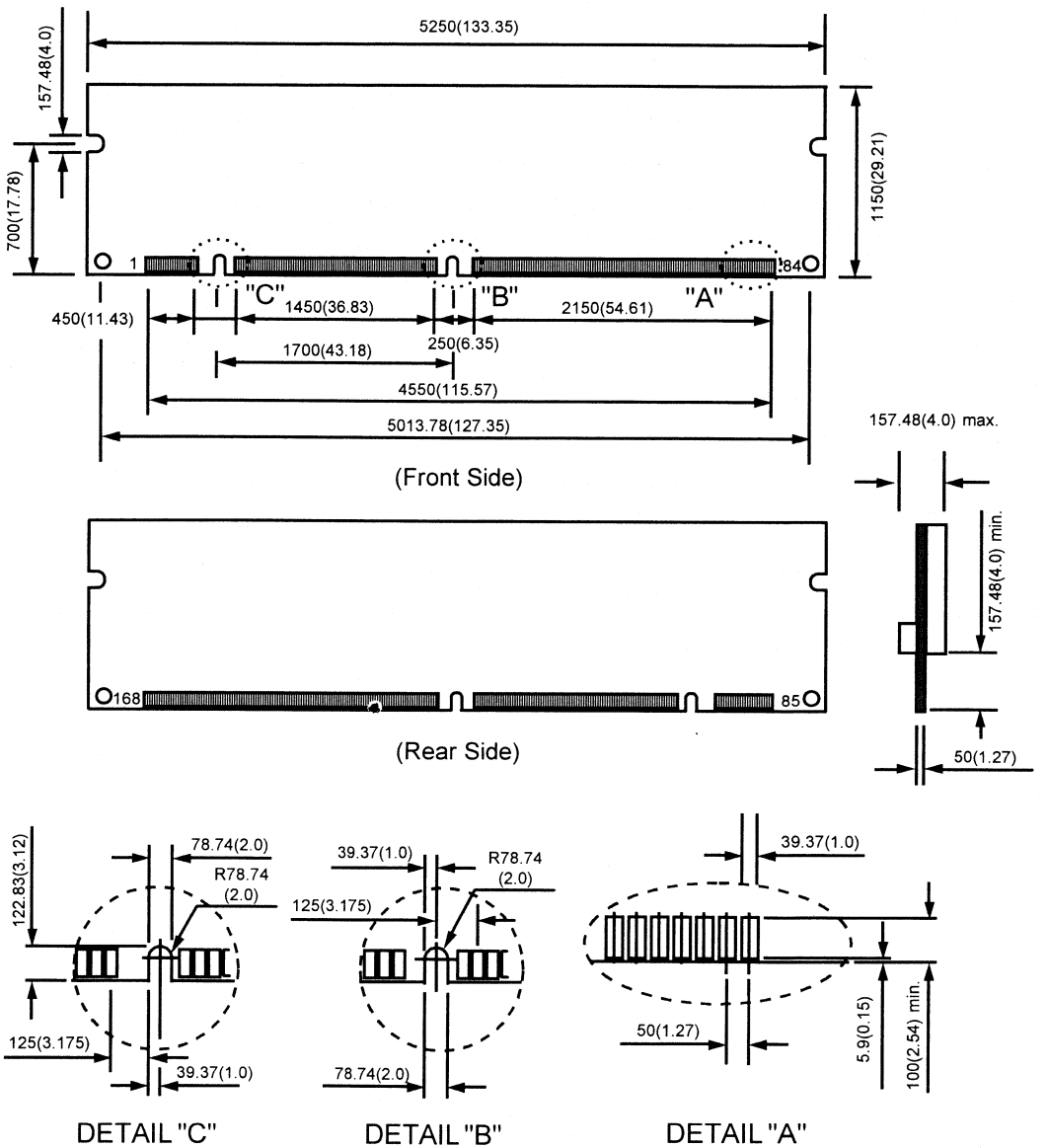
Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-75		-10			-12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



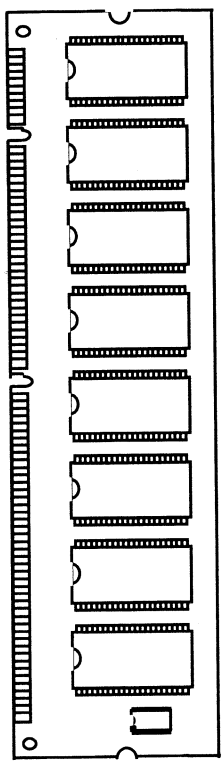
NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

Description

The GMM2644233CTG is a 4M x 64 bits Synchronous Dynamic RAM MODULE which is assembled 16 pieces of 4M x 4bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on an 168 pin printed circuit board with decoupling capacitors. The GMM2644233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2644233CTG provides common data inputs and outputs.

- **GMM2642233CMTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

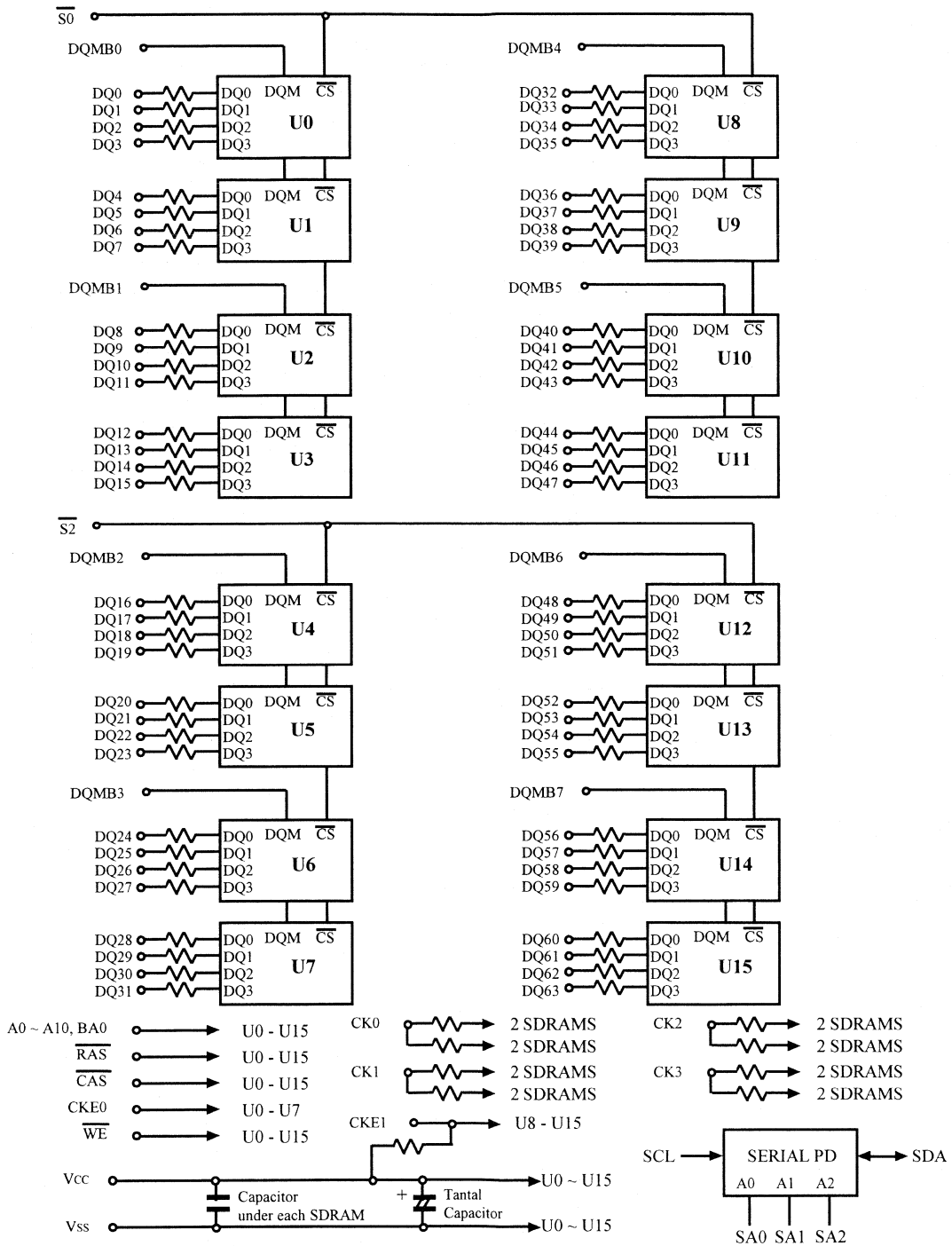
CK0, 1, 2, 3	Clock input
$\overline{CKE0, 1}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	*$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	*$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	NC	49	Vcc	77	DQ31	105	NC	133	Vcc	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	WE	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0, 1 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 2 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x4	04h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Note
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	32MBytes	08h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		1Eh	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2644233CTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			34h	4
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			54h	T
85			47h	G
86			2Dh	-

Byte No.	Function description	Function support	Hex Value	Note
87			31h	1
88			30h	0
89			4Bh	K
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94	Revision Code	YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator's ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's S/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

• Above data are based on the SPD specification of JEDEC standard and can be changed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	16	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	1600	-	1360	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	48	-	48	mA	CKE=V_{IL}, t_{CK}=min	5
			-	32	-	32	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	480	-	400	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	112	-	112	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	560	-	480	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	1600	-	1360	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	2400	-	2000	mA		
Auto Refresh current		I_{CC5}	-	1360	-	1120	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	32	-	32	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-20	20	-20	20	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	Vcc	2.4	Vcc	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	90	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	90	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK3)	-	65	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	50	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	20	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	17	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9.5	-	12		
	(CL=3)	t_{AC}	-	8	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

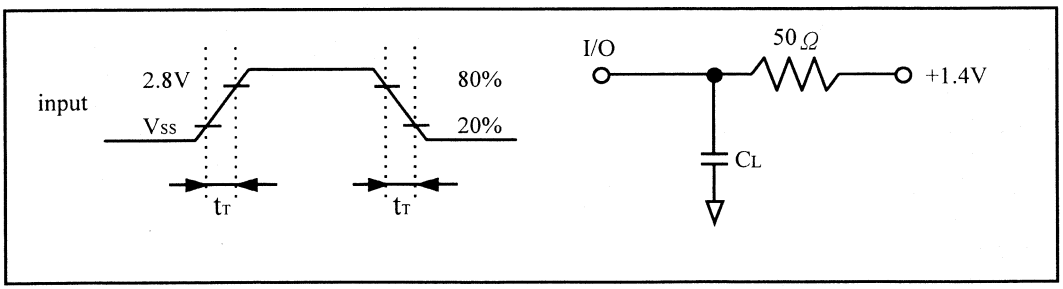
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

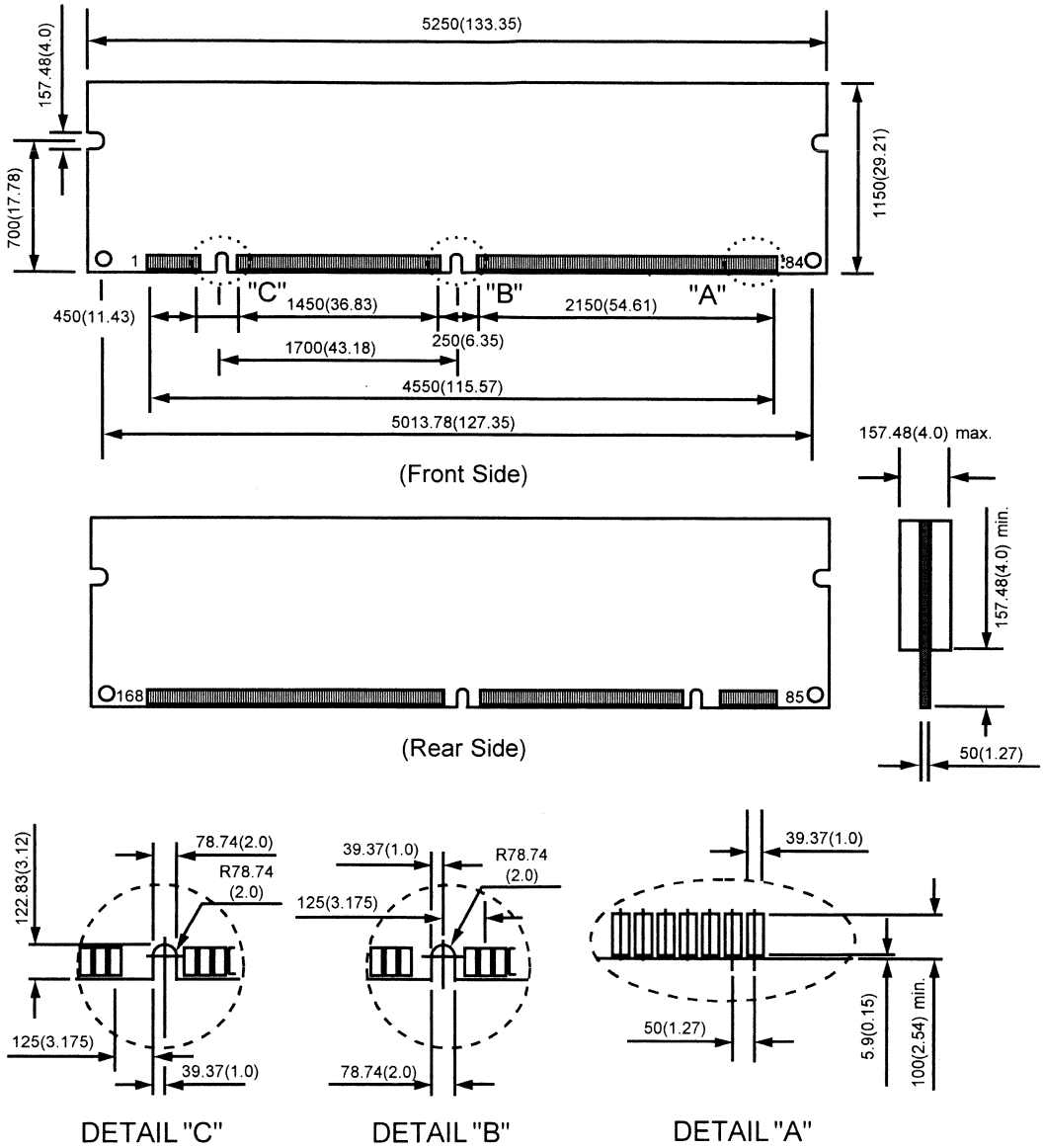
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM2644233CNTG

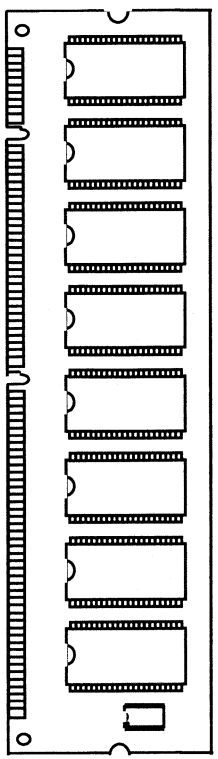
4,194,304 WORDS x 64 BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2644233CNTG is a 4M x 64 bits Synchronous Dynamic RAM MODULE which is assembled 16 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2644233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2644233CNTG provides common data inputs and outputs.

- **GMM2644233CNTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

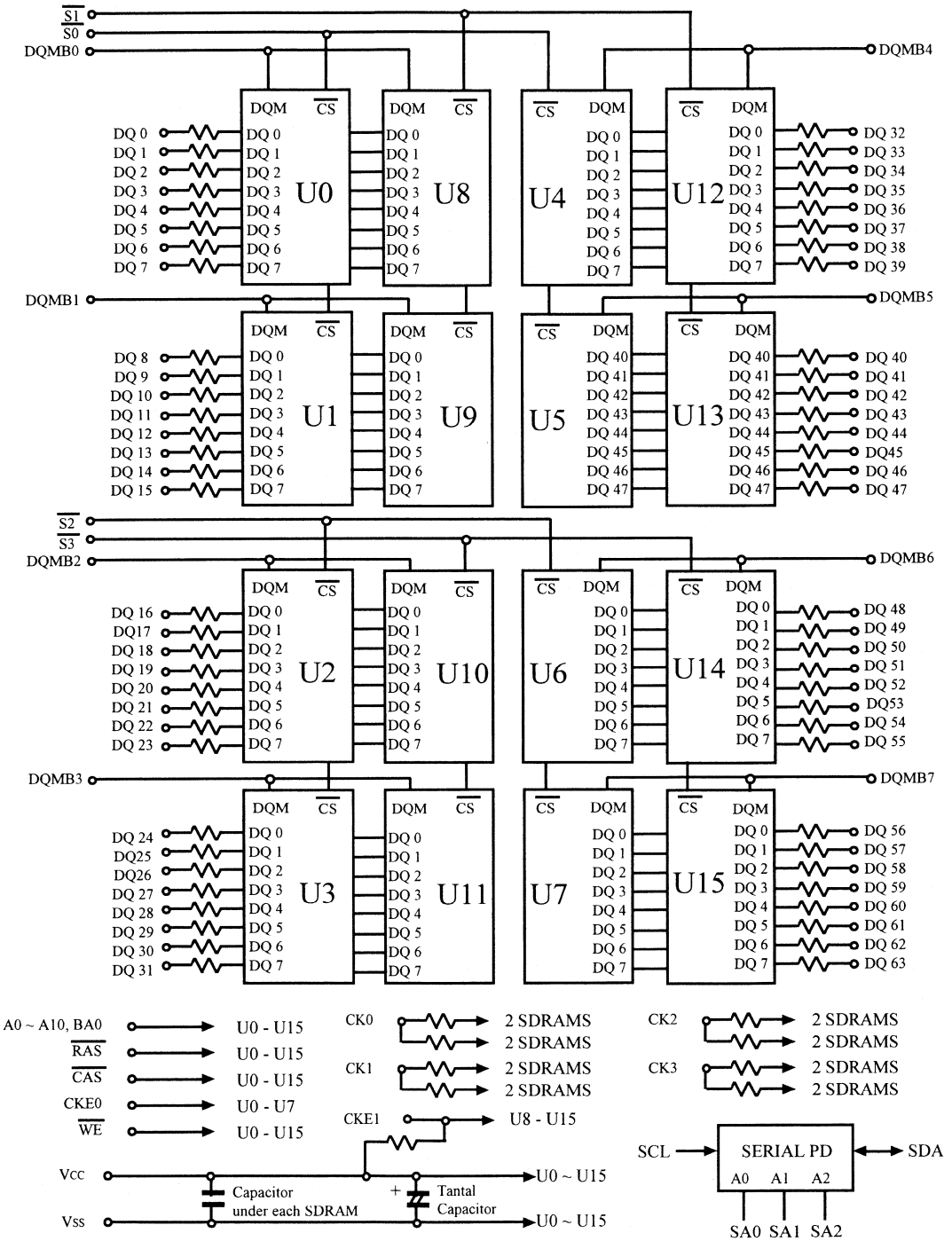
CK0, 1, 2, 3	Clock input
$\overline{CKE0, 1}$	Clock Enable
$\overline{S0, 1, 2, 3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	NC	49	Vcc	77	DQ31	105	NC	133	Vcc	161	DQ63
22	NC	50	NC	78	Vss	106	NC	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	NC	80	NC	108	NC	136	NC	164	NC
25	NC	53	NC	81	NC	109	NC	137	NC	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0, 1 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 1, 2, 3 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
Vcc (power supply pins)	3.3 V is applied. (Vcc is for the internal circuit)
Vss (power supply pins)	Ground is connected. (Vss is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Note
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		1Fh	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2644233CNTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			34h	4
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			4Eh	N
85			54h	T
86			47h	G

Byte No.	Function description	Function support	Hex Value	Note
87			2Dh	-
88			31h	1
89			30h	0
90			4Bh	K
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94	Revision Code	YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator's ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's S/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

• Above data are based on the SPD specification of JEDEC standard and can be changed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	8	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	- 10		- 12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	1080	-	920	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	48	-	48	mA	CKE=V_{IL}, t_{CK}=min	5
			-	32	-	32	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	480	-	400	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	112	-	112	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	560	-	480	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	1080	-	920	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1480	-	1240	mA		
Auto Refresh current		I_{CC5}	-	960	-	800	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	296	-	256	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	95	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	90	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK3)	-	50	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	35	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	25	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	25	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12		
	(CL=3)	t_{AC}	-	7.5	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

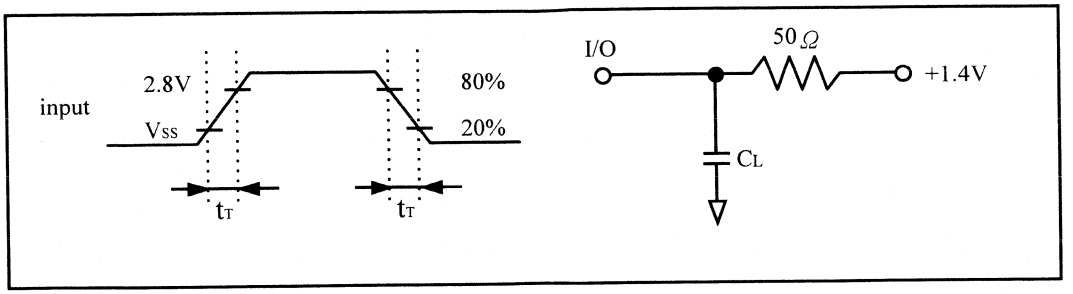
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

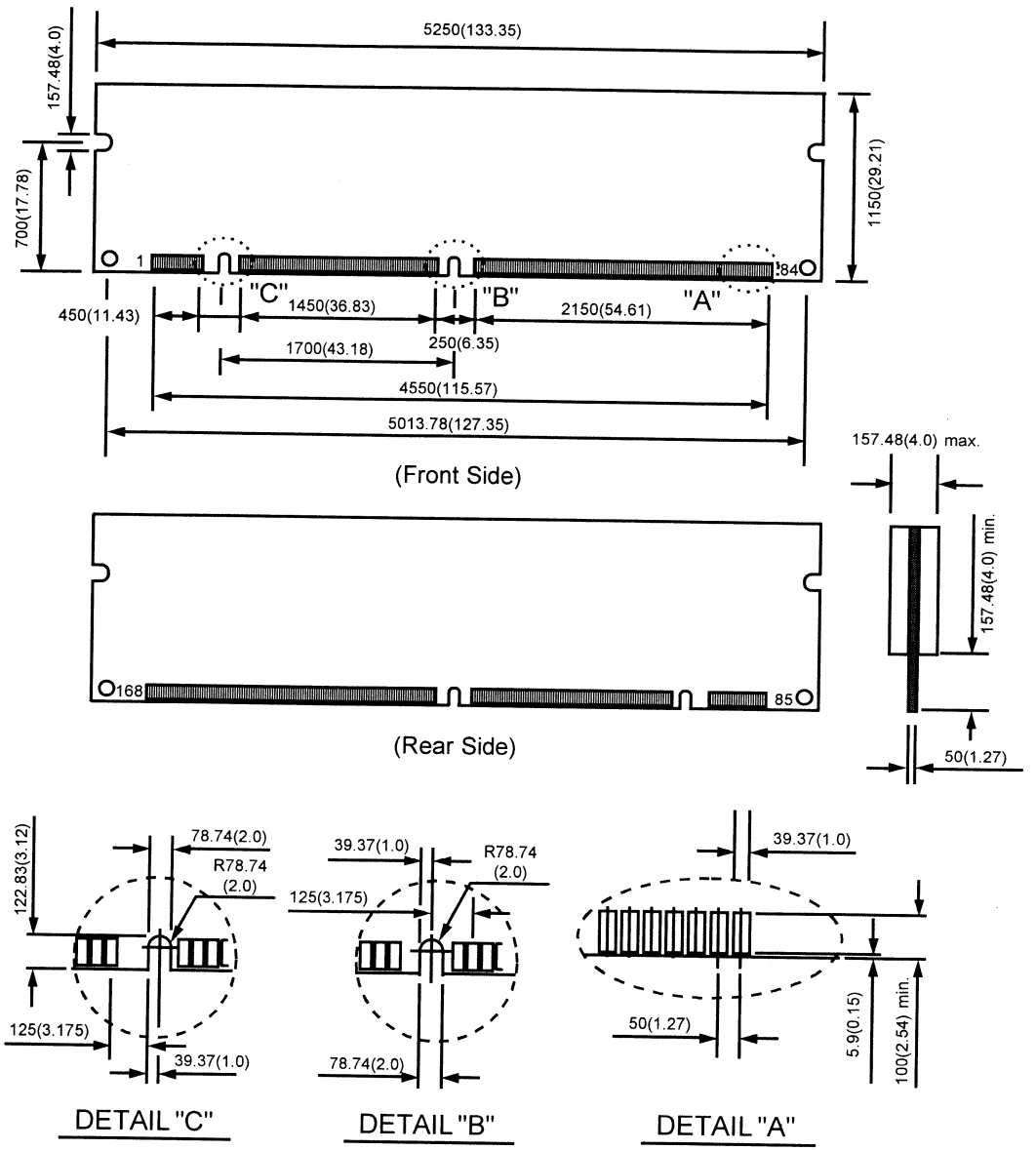
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



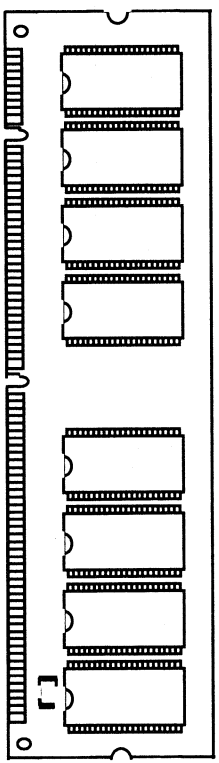
NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

Description

The GMM2644233DNTG is a 4M x 64bits Synchronous Dynamic RAM MODULE which is assembled 16 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2644233DNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2644233DNTG provides common data inputs and outputs.

- **GMM2644233DNTG** (Double Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

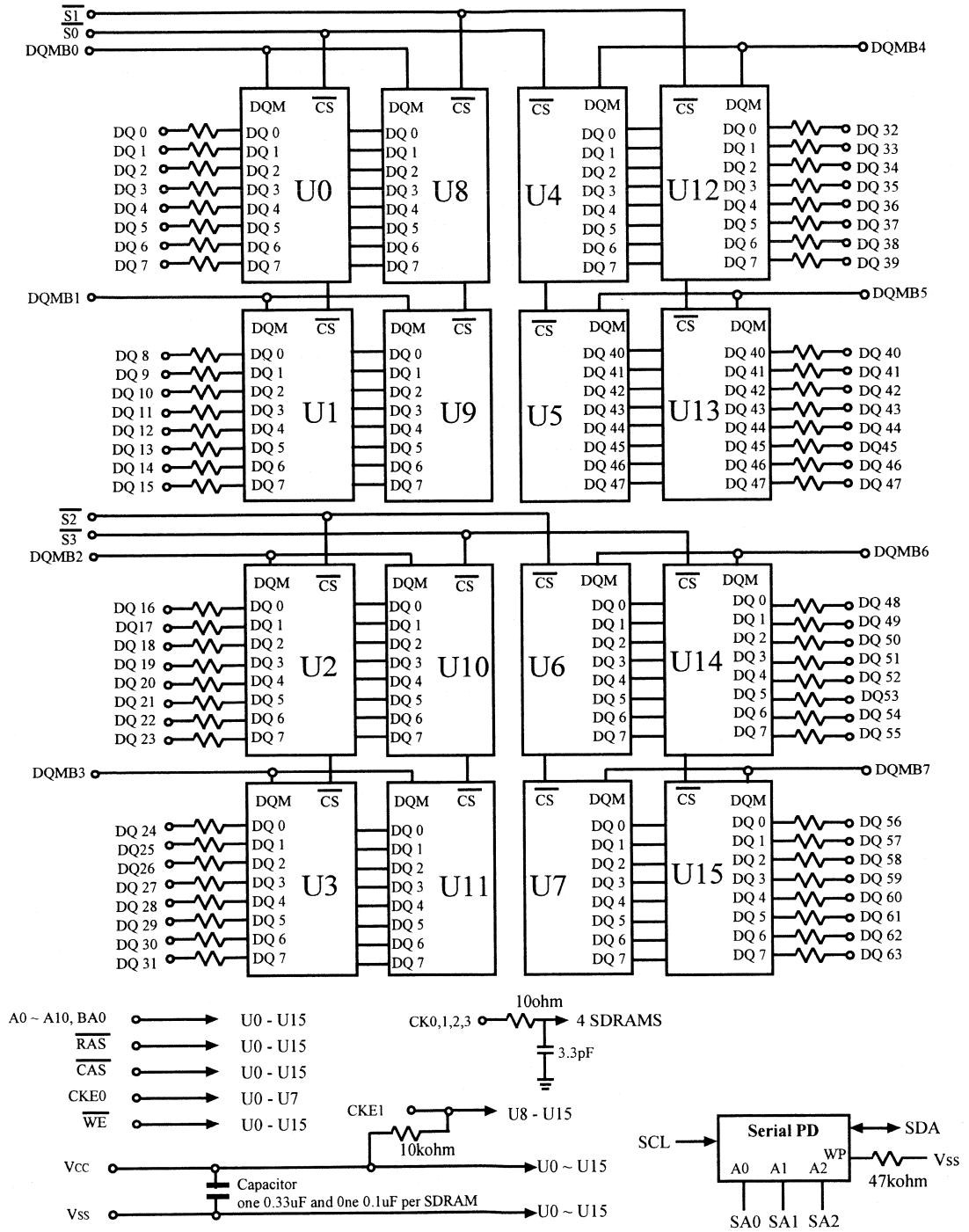
CK0, 1, 2, 3	Clock input
$\overline{CKE0,1}$	Clock Enable
$\overline{S0,1,2,3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0,1,2,3 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=7.5ns	75h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=6.0ns	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=14ns	0Eh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=48ns	30h	
31	Module Bank Density	16MBytes	04h	
32	Command & address signal input setup time	t_{CS} = 2ns	20h	
33	Command & address signal input hold time	t_{CH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1.2	01h	
63	Checksum for bytes 0 ~ 62		B5h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2644233DNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			34h	4
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			44h	D
84			4Dh	N
85			54h	T
86			47h	G
87			2Dh	-
88			37h	7
89			4Ah	J
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-75		-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	1240	-	1120	-	960	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	32	-	48	-	48	mA	CKE=V_{IL}, t_{CK}=min	5
		I_{CC2}	-	32	-	32	-	32	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		(100MHz)	-	640	-	640	-	560	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
		(133MHz)	-	880							
Active standby current (Bank Active)		I_{CC3}	-	112	-	112	-	112	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
		(100MHz)	-	720	-	720	-	640	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
		(133MHz)	-	960							
Burst operating current	(CL=1)	I_{CC4}	-	-	-	720	-	640	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)		-	1520	-	1040	-	920	mA		
	(CL=3)		-	1960	-	1520	-	1280	mA		
Refresh current		I_{CC5}	-	1120	-	1000	-	840	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	443.2	-	336	-	296	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-75		-10		-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

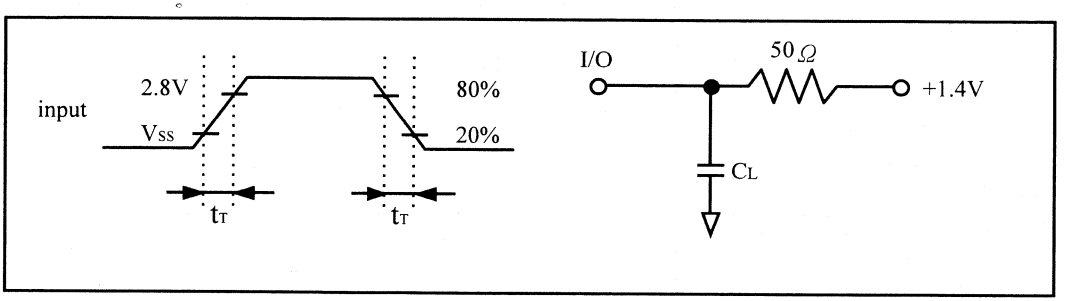
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

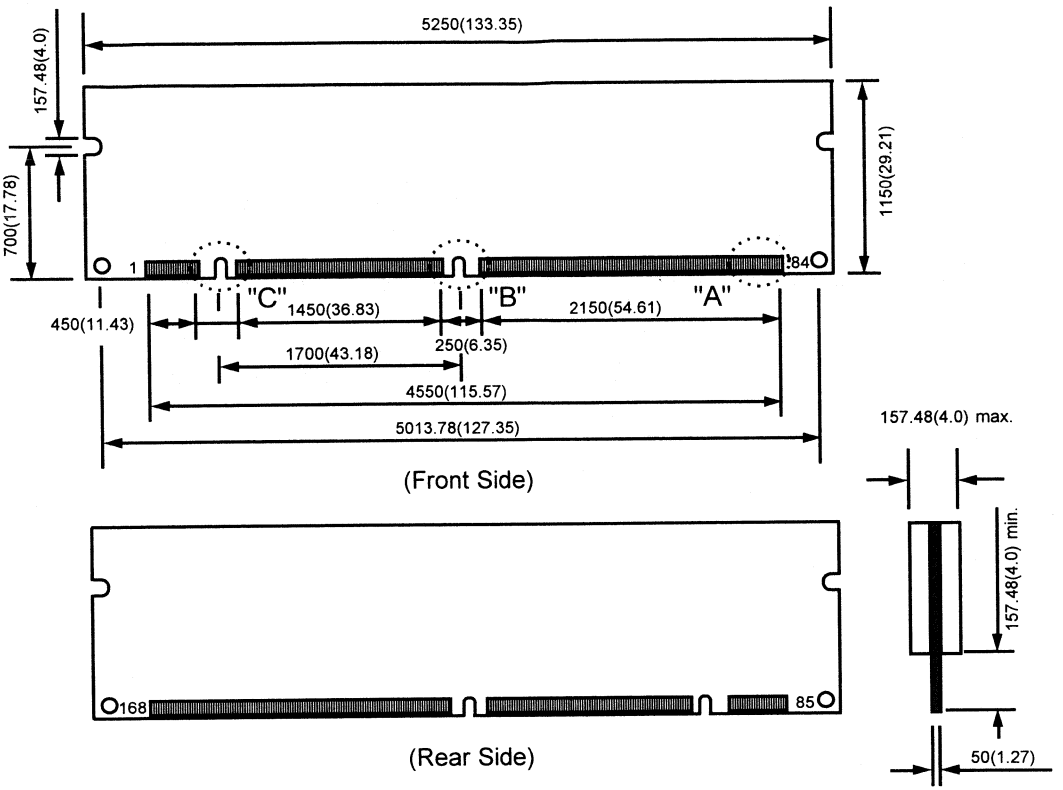
Relationship Between Frequency and Minimum Latency.

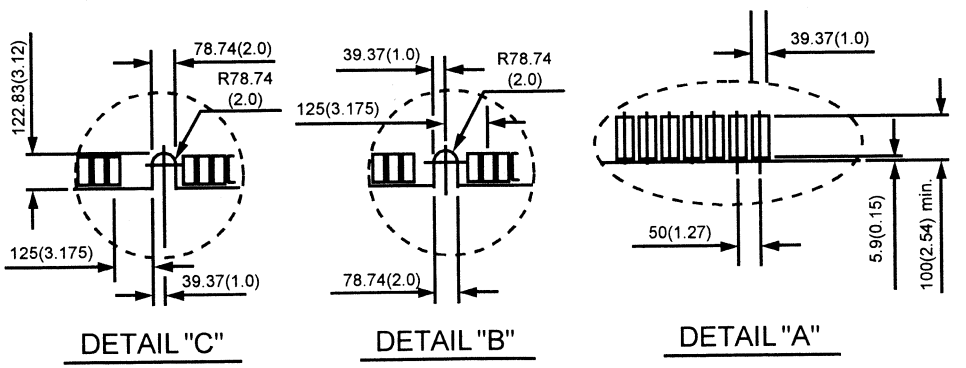
Parameter		Symbol	- 75		- 10			- 12			Notes
Frequency (MHz)			133	100	100	66	33	83	55	28	
t_{CK} (ns)			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)





NOTE : 1. Tolerances on all dimensions ± 5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

LG Semicon Co.,Ltd.

GMM2645233CTG

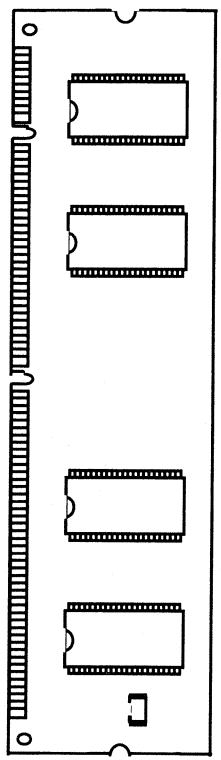
4,194,304 WORDS x64bit
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2645233CTG is a 4M x 64bits Synchronous Dynamic RAM MODULE which is assembled 4 pieces of 4M x 16bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2645233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2645233CTG provides common data inputs and outputs.

- **GMM2645233CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

CK0, 1, 2, 3	Clock input
CKE0	Clock Enable
$\overline{S0,2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

GMM2734233CTG

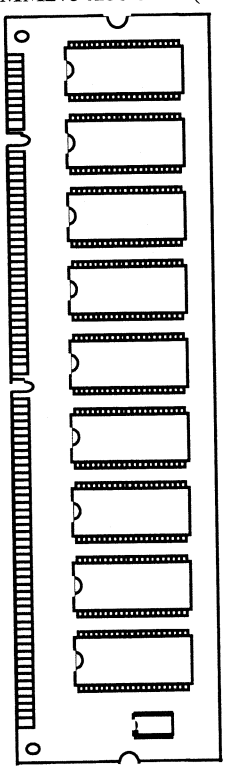
4,194,304 WORDS x 72 BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2734233CTG is a 4M x72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 4M x4bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on an 168 pin printed circuit board with decoupling capacitors. The GMM2734233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2734233CTG provides common data inputs and outputs.

- **GMM2734233CTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
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- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
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  Sequential burst
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- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

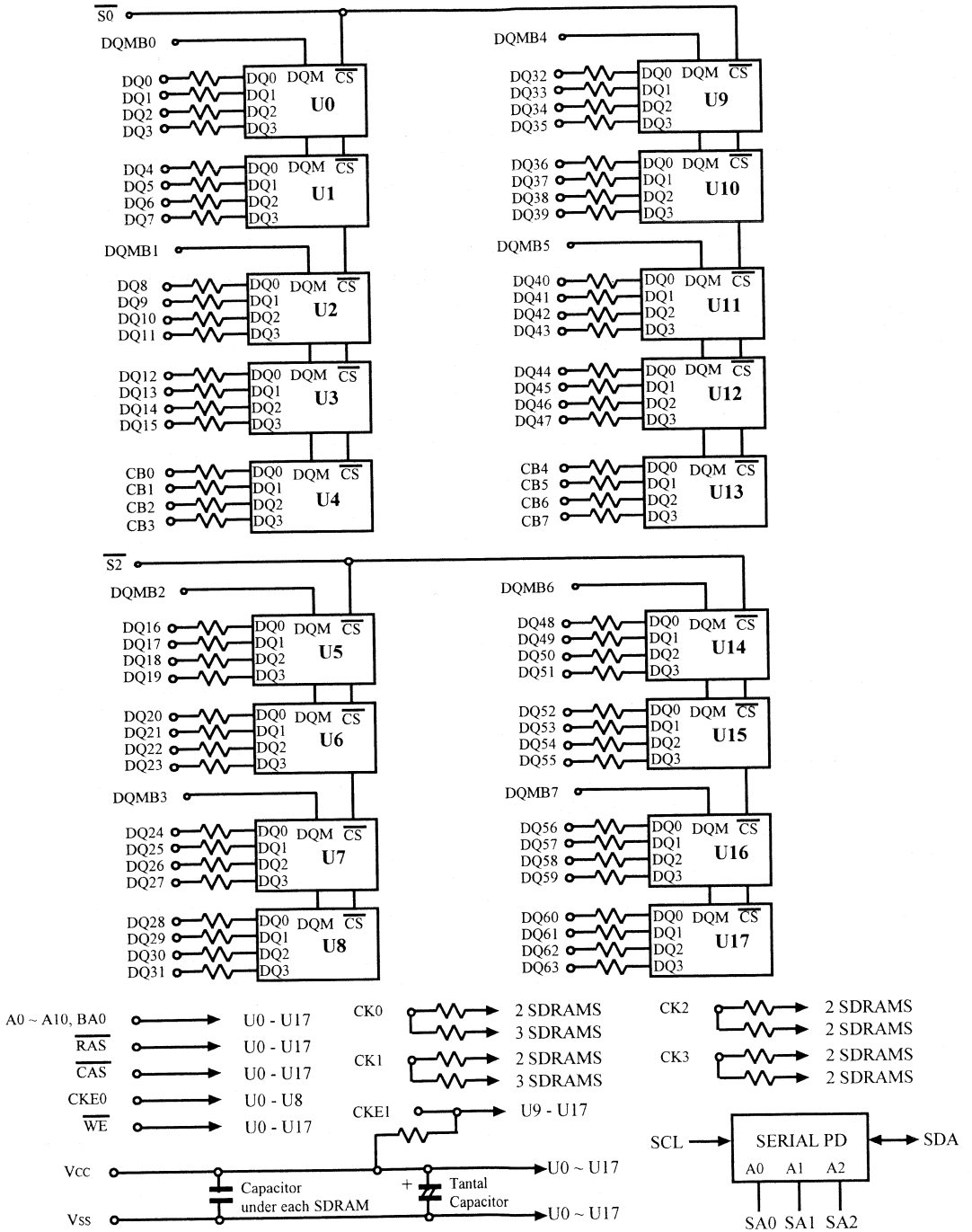
CK0, 1, 2, 3	Clock input
CKE0, 1	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	$\overline{Vcc}$	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0, 1 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 2 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x4	04h	
14	Error checking DRAM data width	x4	04h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Note
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	32MBytes	08h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		2Ch	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	00h	
66~71			E0h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2734233CTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			34h	4
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			54h	T
85			47h	G
86			2Dh	-

Byte No.	Function description	Function support	Hex Value	Note
87			31h	1
88			30h	0
89			4Bh	K
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94	Revision Code	YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator's ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's S/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

• Above data are based on the SPD specification of JEDEC standard and can be changed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	18	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	1800	-	1530	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	54	-	54	mA	CKE=V_{IL}, t_{CK}=min	5
			-	36	-	36	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	560	-	470	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	126	-	126	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	630	-	540	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	1800	-	1530	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	2700	-	2250	mA		
Auto Refresh current		I_{CC5}	-	1530	-	1260	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	36	-	36	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	Vcc	2.4	Vcc	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	100	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	100	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK3)	-	75	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	55	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	25	pF	1, 3
$C_{I/O}$	I/O capacitance (DQ0 ~ DQ63, CB0 ~ 7)	-	15	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-10		-12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9.5	-	12		
	(CL=3)	t_{AC}	-	8	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

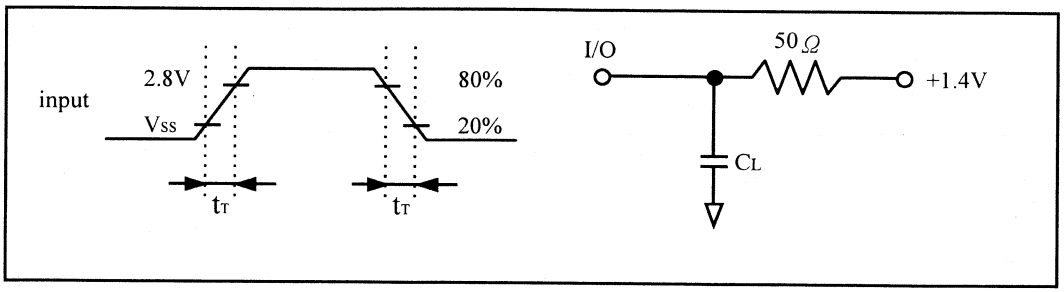
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

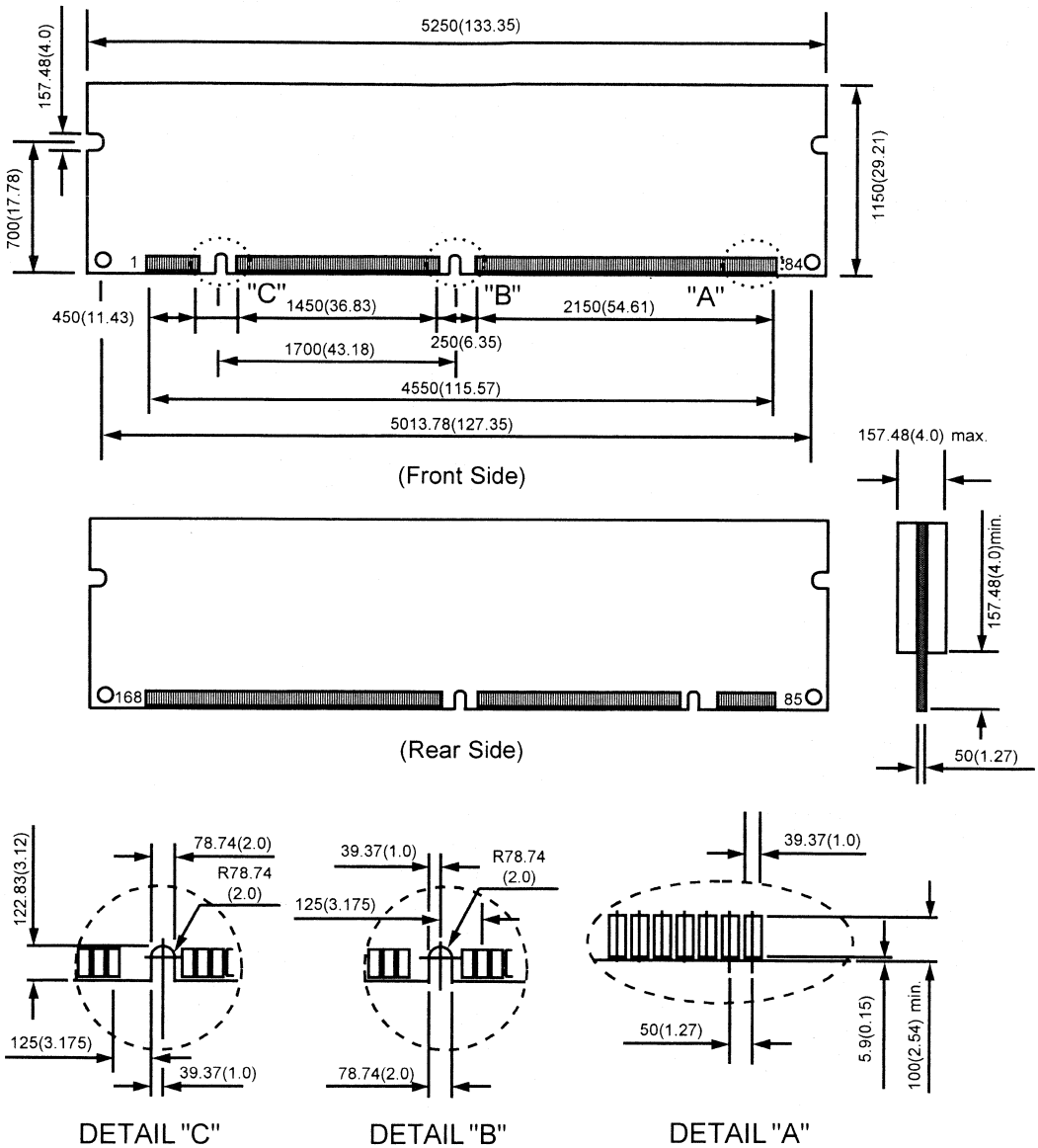
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM2734233CNTG

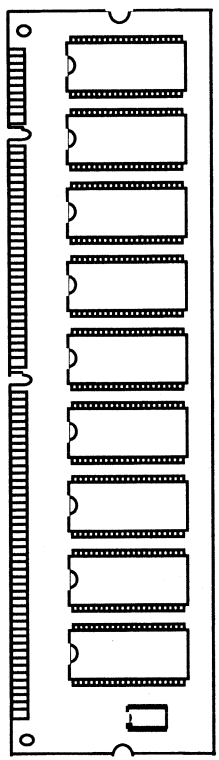
4,194,304 WORDS x 72 BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2734233CNTG is a 4M x 72 bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2734233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2734233CNTG provides common data inputs and outputs.

- **GMM2734233CNTG** (Both Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

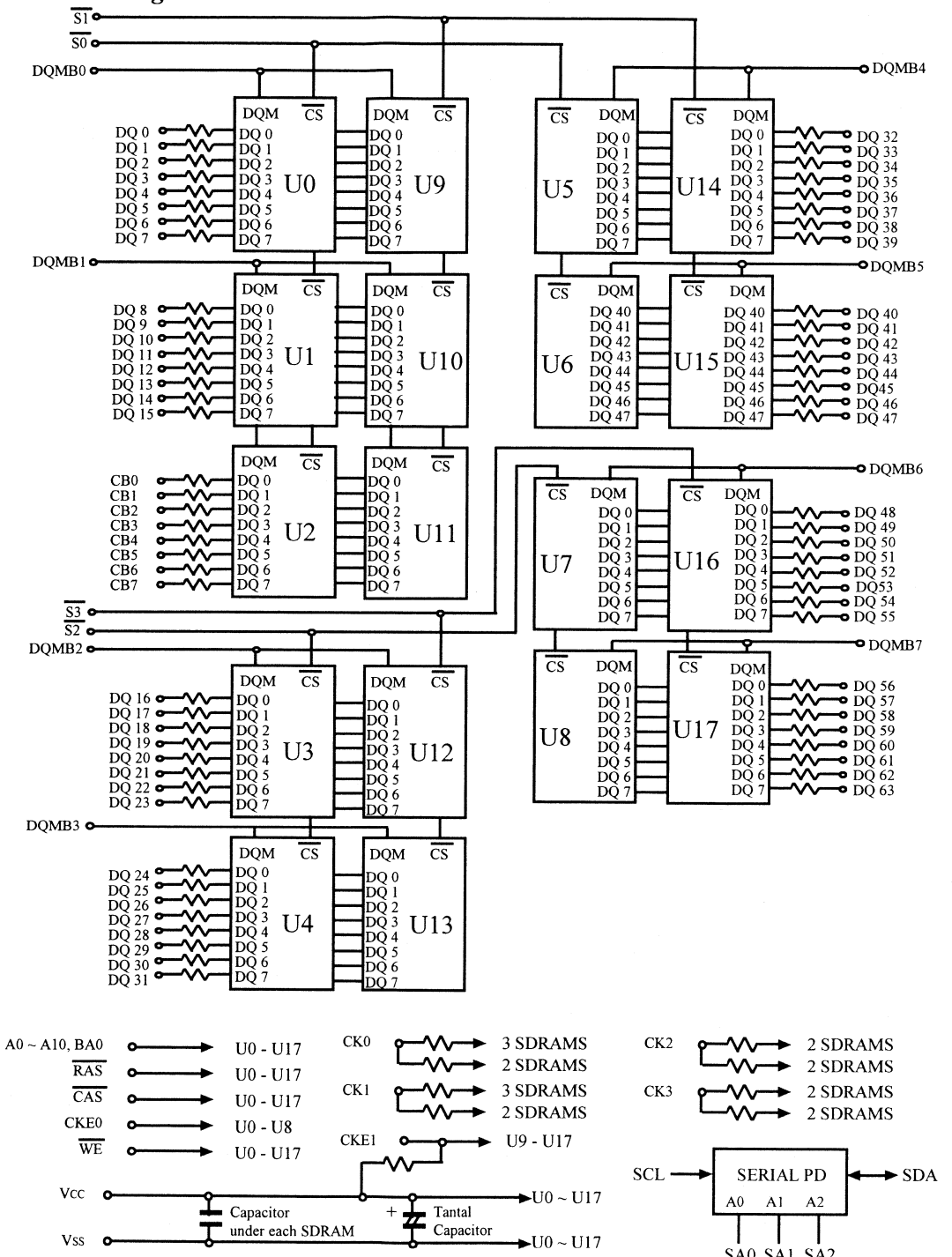
CK0, 1, 2, 3	Clock input
$\overline{CKE0, 1}$	Clock Enable
$\overline{S0, 1, 2, 3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
CB0 ~ 7	Check Bits
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	NC	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0, 1 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0, 1, 2, 3 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=7.5ns	75h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Note
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		31h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	00h	
66~71			E0h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2734233CNTG-10K	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			34h	4
80			32h	2
81			33h	3
82			33h	3
83			43h	C
84			4Eh	N
85			54h	T
86			47h	G

Byte No.	Function description	Function support	Hex Value	Note
87			2Dh	-
88			31h	1
89			30h	0
90			4Bh	K
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94	Revision Code	YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification frequency	66MHz	66h	
127	Intel specification CAS# Latency Support		06h	
128~135	System Integrator's ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's S/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

• Above data are based on the SPD specification of JEDEC standard and can be changed.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	9	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	- 10		- 12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	1215	-	1035	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	54	-	54	mA	CKE=V_{IL}, t_{CK}=min	5
			-	36	-	36	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	540	-	450	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	126	-	126	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	630	-	540	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	1215	-	1035	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1665	-	1395	mA		
Auto Refresh current		I_{CC5}	-	1080	-	900	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	333	-	288	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	Vcc	2.4	Vcc	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	100	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	95	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK3)	-	50	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	35	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	25	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	25	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-10		-12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9	-	12		
	(CL=3)	t_{AC}	-	7.5	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

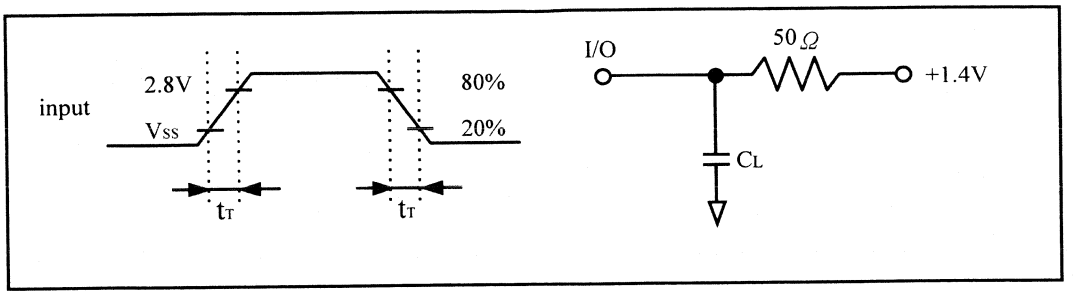
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

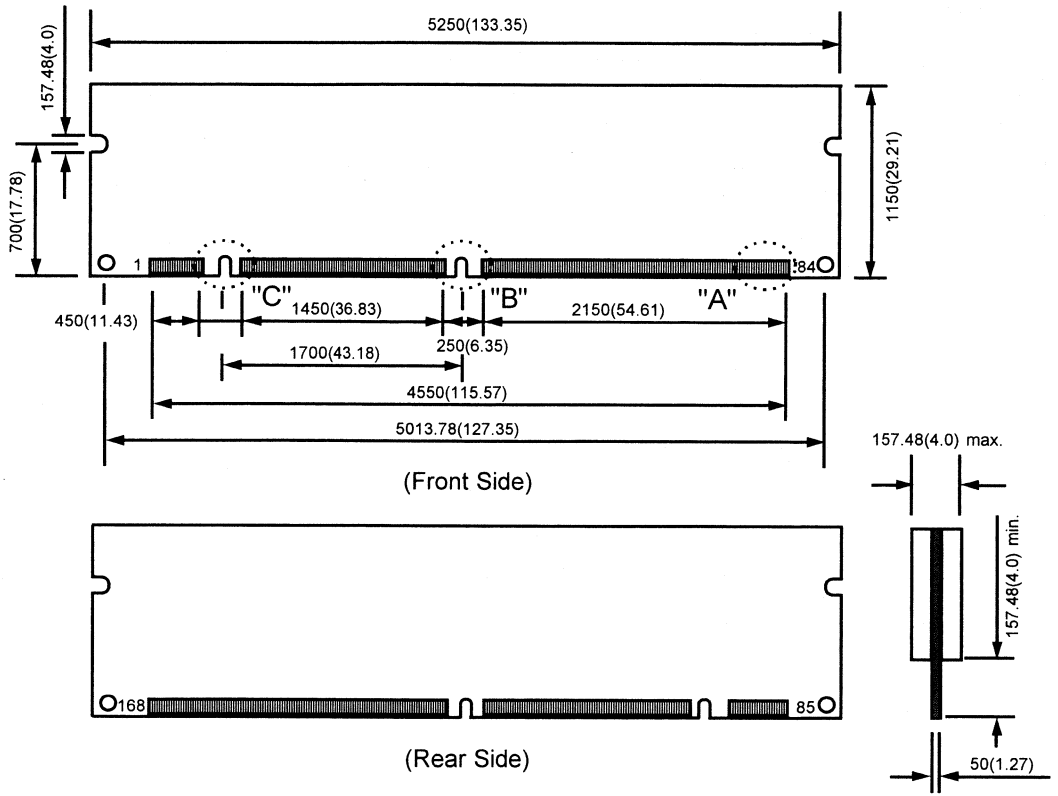
Relationship Between Frequency and Minimum Latency. (Continued)

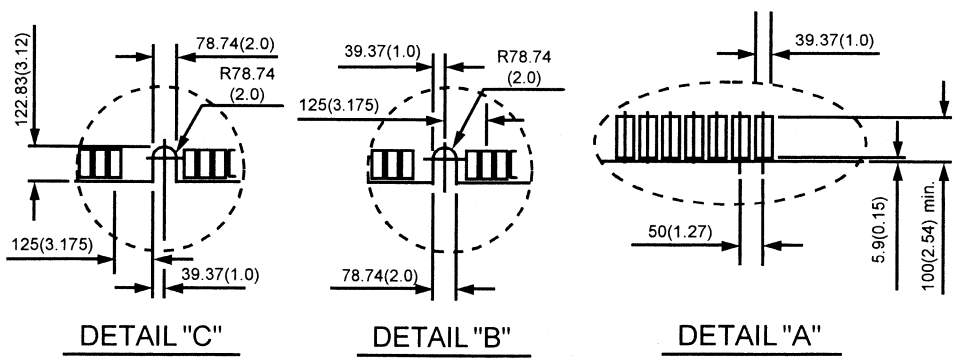
Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)





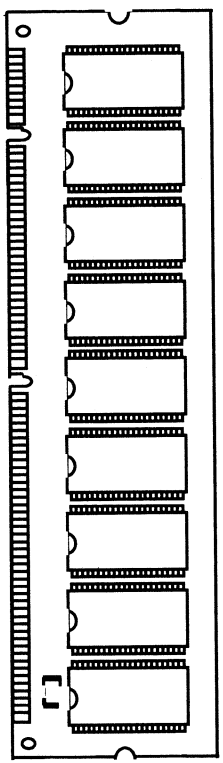
NOTE : 1. Tolerances on all dimensions ± 5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

Description

The GMM2734233DNTG is a 4M x 72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2734233DNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2734233DNTG provides common data inputs and outputs.

- **GMM2734233DNTG** (Double Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

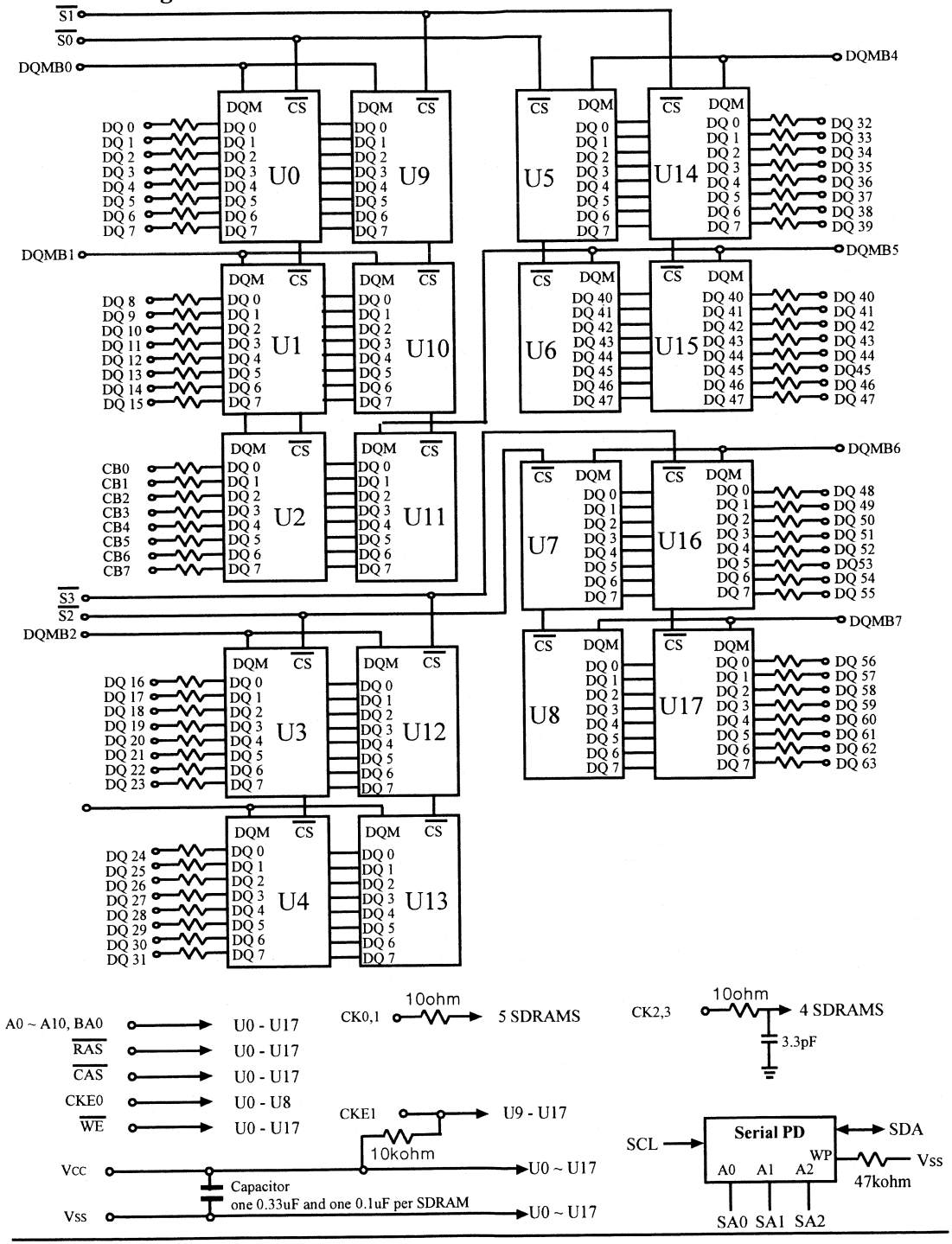
CK0, 1, 2, 3	Clock input
CKE0,1	Clock Enable
$\overline{S0,1,2,3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A10	Address input
BA0	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	*BA1	67	DQ23	95	DQ40	123	*A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0,1,2,3 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=7.5ns	75h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	2 banks	02h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=10ns	A0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=6.0ns	60h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=14ns	0Eh	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=48ns	30h	
31	Module Bank Density	16MBytes	04h	
32	Command & address signal input setup time	t_{CS} = 2ns	20h	
33	Command & address signal input hold time	t_{CH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
36~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		C7h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2734233DNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			34h	4
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			44h	D
84			4Dh	N
85			54h	T
86			47h	G
87			2Dh	-
88			37h	7
89			4Ah	J
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-1.0 to +4.6	V	1
Supply voltage relative to Vss	V_{CC}	-1.0 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	- 75		- 10		- 12		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current		I_{CC1}	-	1395	-	1260	-	1080	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	36	-	54	-	54	mA	CKE=V_{IL}, t_{CK}=min	5
		I_{CC2}	-	36	-	36	-	36	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		(100MHz)	-	720	-	720	-	630	mA	CKE=V_{IH}, NOP command t_{CK}=min	3
		(133MHz)	-	990							
Active standby current (Bank Active)		I_{CC3}	-	126	-	126	-	126	mA	CKE=V_{IL}, t_{CK}=min, I/O = High-Z	1, 2
		(100MHz)	-	810	-	810	-	720	mA	CKE=V_{IH}, NOP command t_{CK}=min, I/O = High-Z	1, 2, 3
		(133MHz)	-	1080							
Burst operating current	(CL=1)	I_{CC4}	-	-	-	810	-	720	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=2)		-	1710	-	1170	-	1035	mA		
	(CL=3)		-	2205	-	1710	-	1440	mA		
Refresh current		I_{CC5}	-	1260	-	1125	-	945	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	498.6	-	378	-	333	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	-10	10	μA	0≤Vin≤Vcc	
Output leakage current		I_{LO}	-10	10	-10	10	-10	10	μA	0≤Vout≤Vcc I/O = disable	
Output high voltage		V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is one per one CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB1, DQMB5)	-	TBD	pF	1, 2
C_{I6}	Input capacitance (DQMB0, 2, 3, 4, 6, 7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 75		- 10		- 12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	-	-	30	-	36	-	ns	1
	(CL=2)	t_{CK}	10	-	15	-	18	-		
	(CL=3)	t_{CK}	7.5	-	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	-	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	6	-	9	-	12		
	(CL=3)	t_{AC}	-	6	-	7.5	-	9		
Data-out hold time		t_{OH}	3	-	3	-	3	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	0	-	0	-	0	-	ns	1, 2, 3
CLK to Data-out high impedence	(CL=1)	t_{HZ}	-	-	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	6	-	7	-	9		
Data-in setup time		t_{DS}	2	-	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	3	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	3	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	90	-	100	-	ns	1
Active to Precharge command period		t_{RAS}	48	120000	60	120000	70	120000	ns	1

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

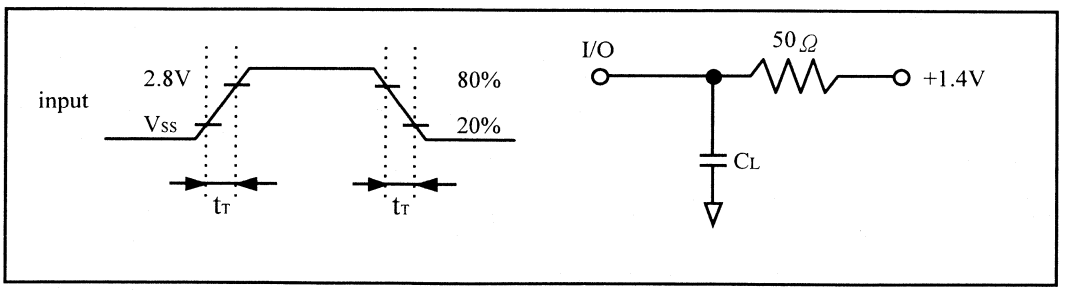
Parameter	Symbol	- 75		- 10		- 12		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	20	-	30	-	30	-	ns	1
Precharge to active command period	t_{RP}	20	-	30	-	30	-	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	10	-	15	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	14	-	20	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.
6. -10 grade products are classified as follows.
   ① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.
   ② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.
   ③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-75		-10			-12			Notes
			133	100	100	66	33	83	55	28	
			7.5	10	10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	3	2	1	3	2	1	1
Active command to active command period (same bank)		t_{RC}	10	7	9	6	3	9	6	3	= [t_{RAS} +t_{RP}], 1
Active command to precharge command (same bank)		t_{RAS}	7	5	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	3	2	1	3	2	1	1
Write recovery or data-in to precharge command (same bank)		t_{DPL}	2	1	2	1	1	2	1	1	1
Active command to active command (different bank)		t_{RRD}	2	2	2	2	1	2	2	1	1
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	5	3	2	5	3	2	= [t_{RWL} +t_{RP}], 1
Self refresh exit to command input		I_{SEC}	9	6	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedence	(CL=3)	I_{HZP}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	2	2	

Relationship Between Frequency and Minimum Latency.

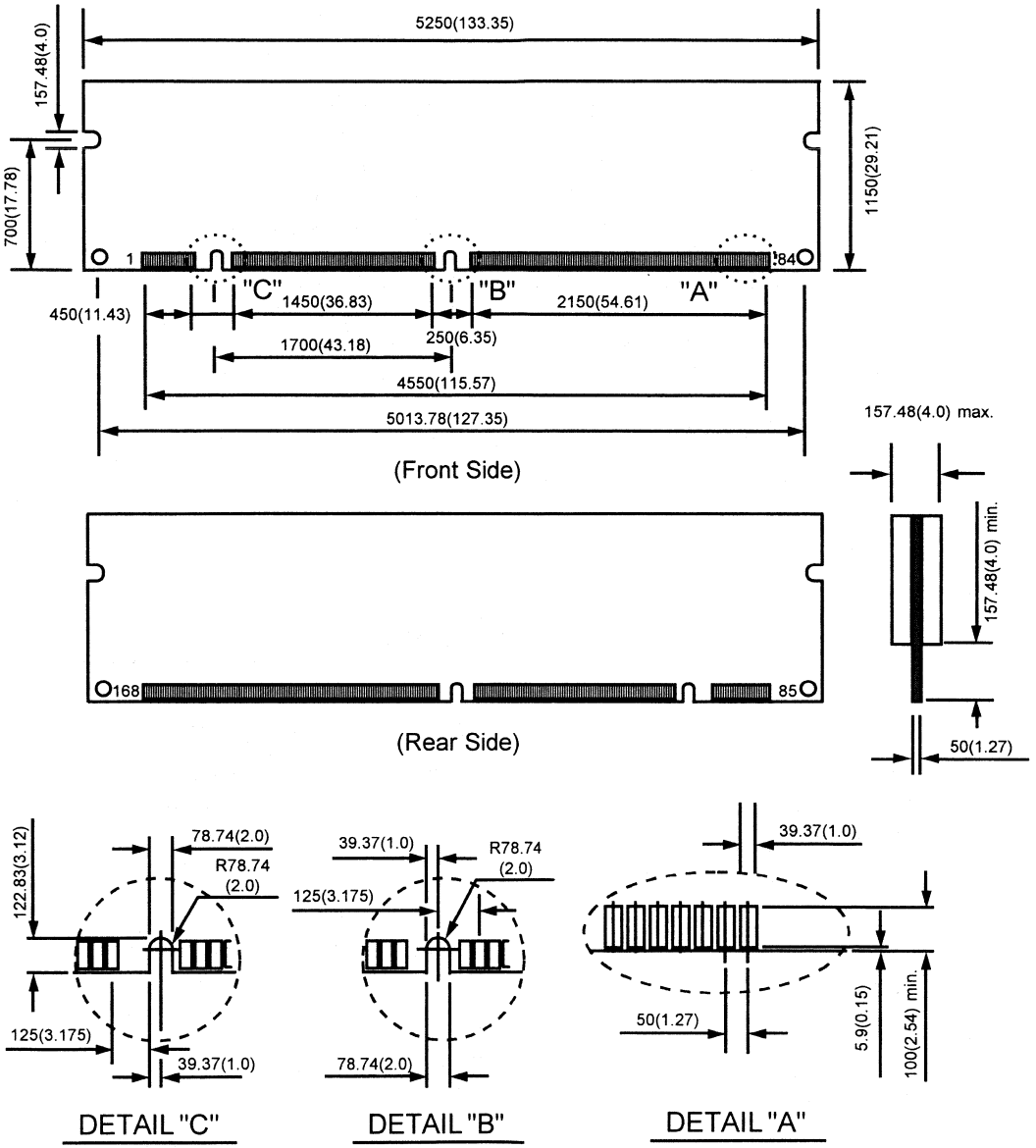
Parameter / Frequency (MHz) / t_{CK} (ns)		Symbol	-75		-10			-12			Notes
			133	100	100	66	33	83	55	28	
			7.5	10	10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	-	-	0	-	-	0	
Burst stop to output high impedence	(CL=3)	I_{BSH}	3	3	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.

2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

LG Semicon Co.,Ltd.

GMM2735233CTG

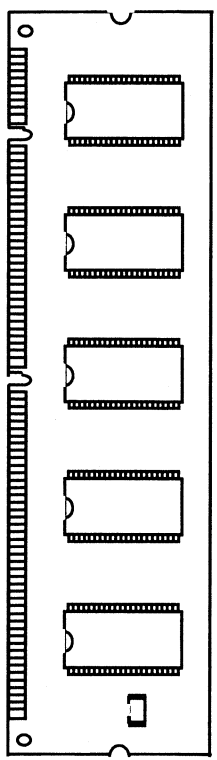
4,194,304 WORDS x64bit
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2735233CTG is a 4M x 72bits Synchronous Dynamic RAM MODULE which is assembled 5 pieces of 4M x 16bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2735233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2735233CTG provides common data inputs and outputs.

- **GMM2735233CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

CK0, 1, 2, 3	Clock input
CKE0	Clock Enable
$\overline{S0,2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

GMM2649233CTG

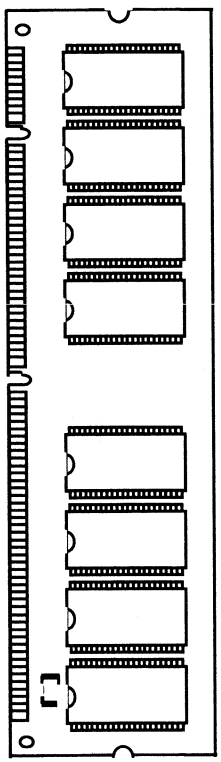
8,388,608 WORDS x64bit
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2649233CTG is a 8M x 64bits Synchronous Dynamic RAM MODULE which is assembled 8 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2649233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2649233CTG provides common data inputs and outputs.

- **GMM2649233CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
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- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
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  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

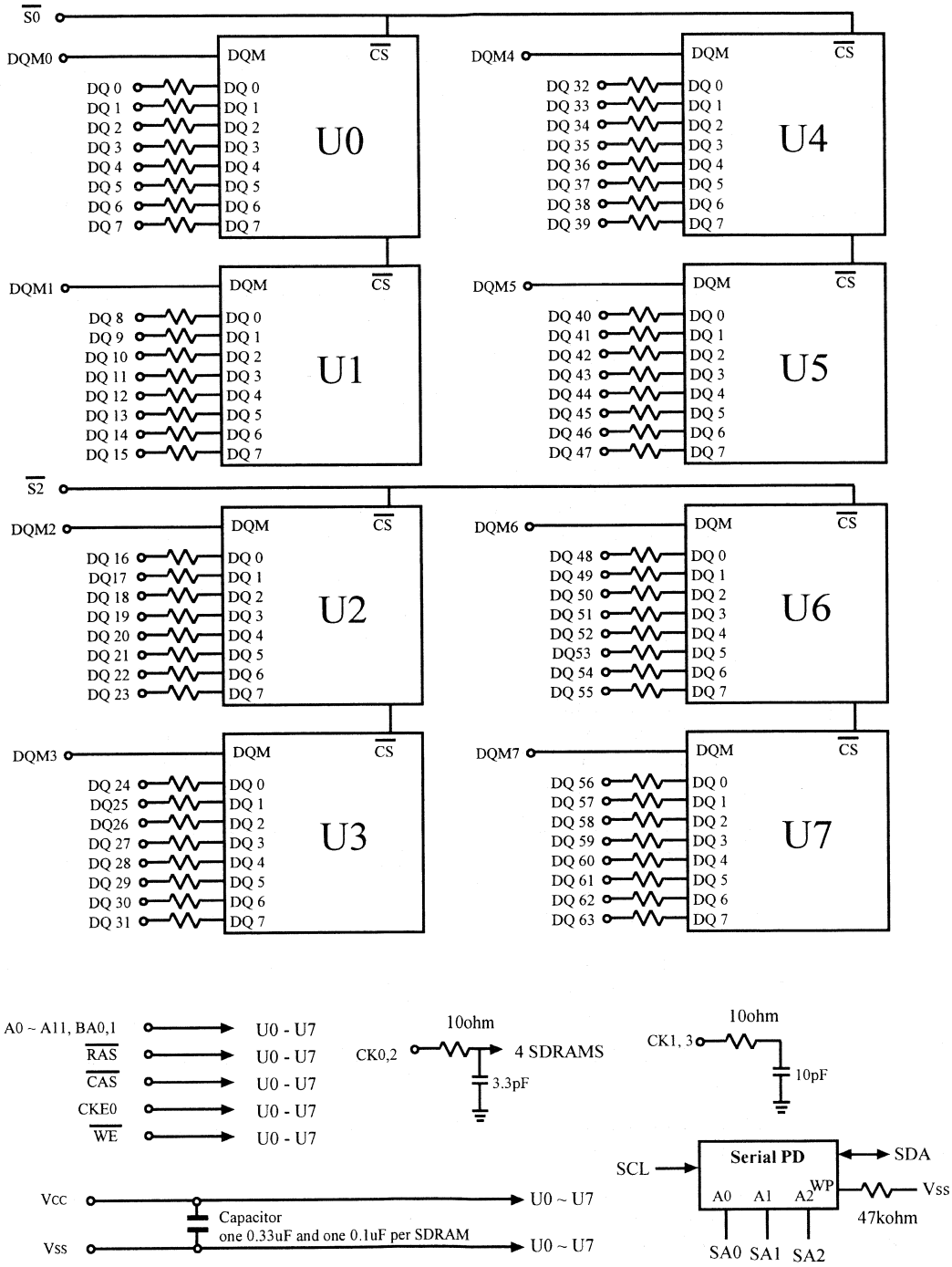
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=7.0ns	70h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=50ns	32h	
31	Module Bank Density	64MBytes	10h	
32	Command & address signal input setup time	t_{AS} = 2ns	20h	
33	Command & address signal input hold time	t_{AH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		56h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2649233CTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			39h	9
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			43h	C
84			54h	T
85			47h	G
86			2Dh	-
87			37h	7
88			4Ah	J
89			20h	
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		AFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, V_{SS}, V_{SSQ}= 0 V)
(GM72V66841CT)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	480	-	520	-	400	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	640	-	680	-	560	mA		
Standby current in power down		I_{CC2P}	-	24	-	24	-	24	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	16	-	16	-	16	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	160	-	160	-	160	mA	CKE,CS = V_{IL}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	72	-	72	-	72	mA	CKE = V_{IL}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	48	-	48	-	48	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	40	-	40	-	40	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	240	-	240	-	240	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	160	-	160	-	160	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	560	-	760	-	560	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	960	-	1240	-	960	mA		
Refresh current	(CL= 2)	I_{CC5}	-	640	-	680	-	480	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	1040	-	1120	-	880	mA		
Self refresh current		I_{CC6}	-	16	-	16	-	16	mA	V_{IH} ≥ V_{CC} - 0.2 V_{IL} ≤0.2V	7

Parameter	Symbol	- 7		- 8		- 10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq Vcc$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq Vcc$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

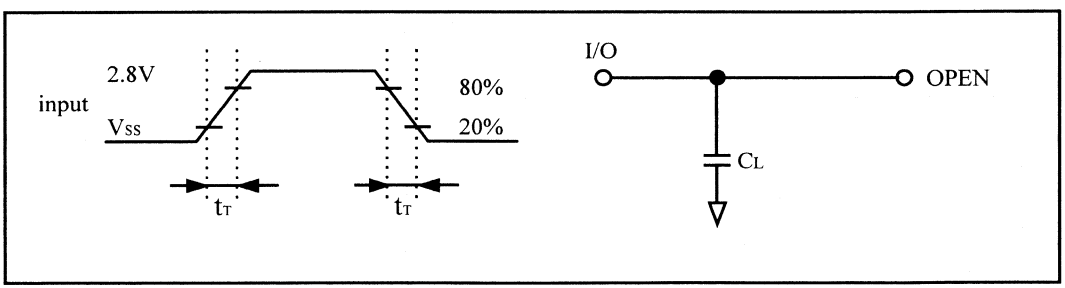
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Active command to column command (same bank)		l_{RCD}	3	2	3	2	3	2	1
Active command to active command period (same bank)		l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)		l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)		l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)		l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)		l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time		l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)		l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input		l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence	(CL=2)	l_{HZP}	-	2	-	2	-	2	
	(CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)		l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=2)	l_{EP}	-	-1	-	-1	-	-1	
	(CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	
Column command to column command		l_{CCD}	1	1	1	1	1	1	
Write command to data in latency		l_{WCD}	0	0	0	0	0	0	
DQM to data in		l_{DID}	0	0	0	0	0	0	
DQM to data out		l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable		l_{CLE}	1	1	1	1	1	1	
Register set to active command		l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable		l_{CDD}	0	0	0	0	0	0	
Power down exit to command input		l_{PEC}	1	1	1	1	1	1	

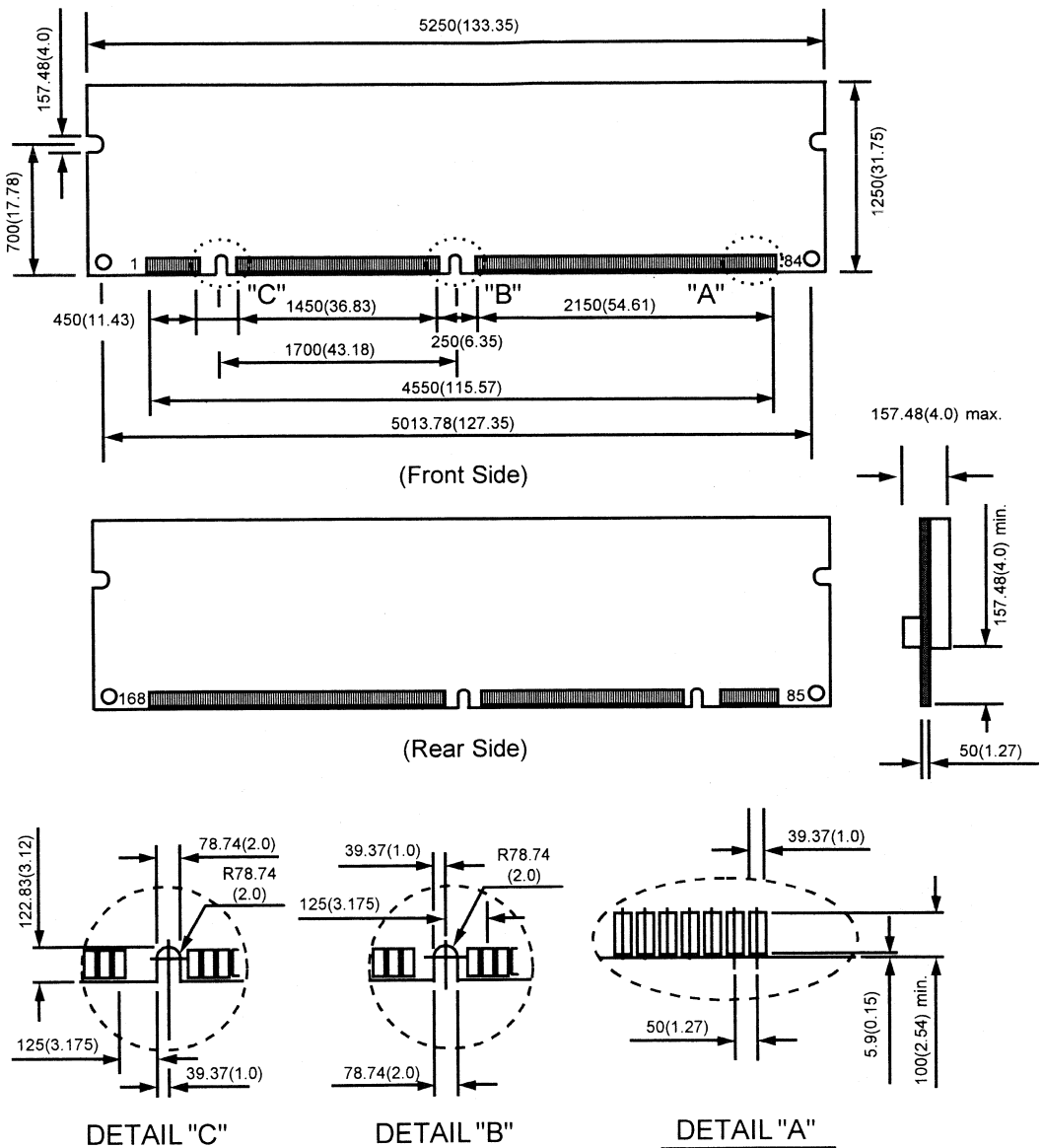
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM2739233CTG

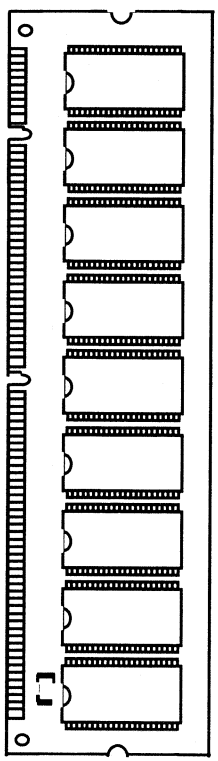
8,388,608 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2739233CTG is a 8M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2739233CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2739233CTG provides common data inputs and outputs.

- **GMM2739233CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

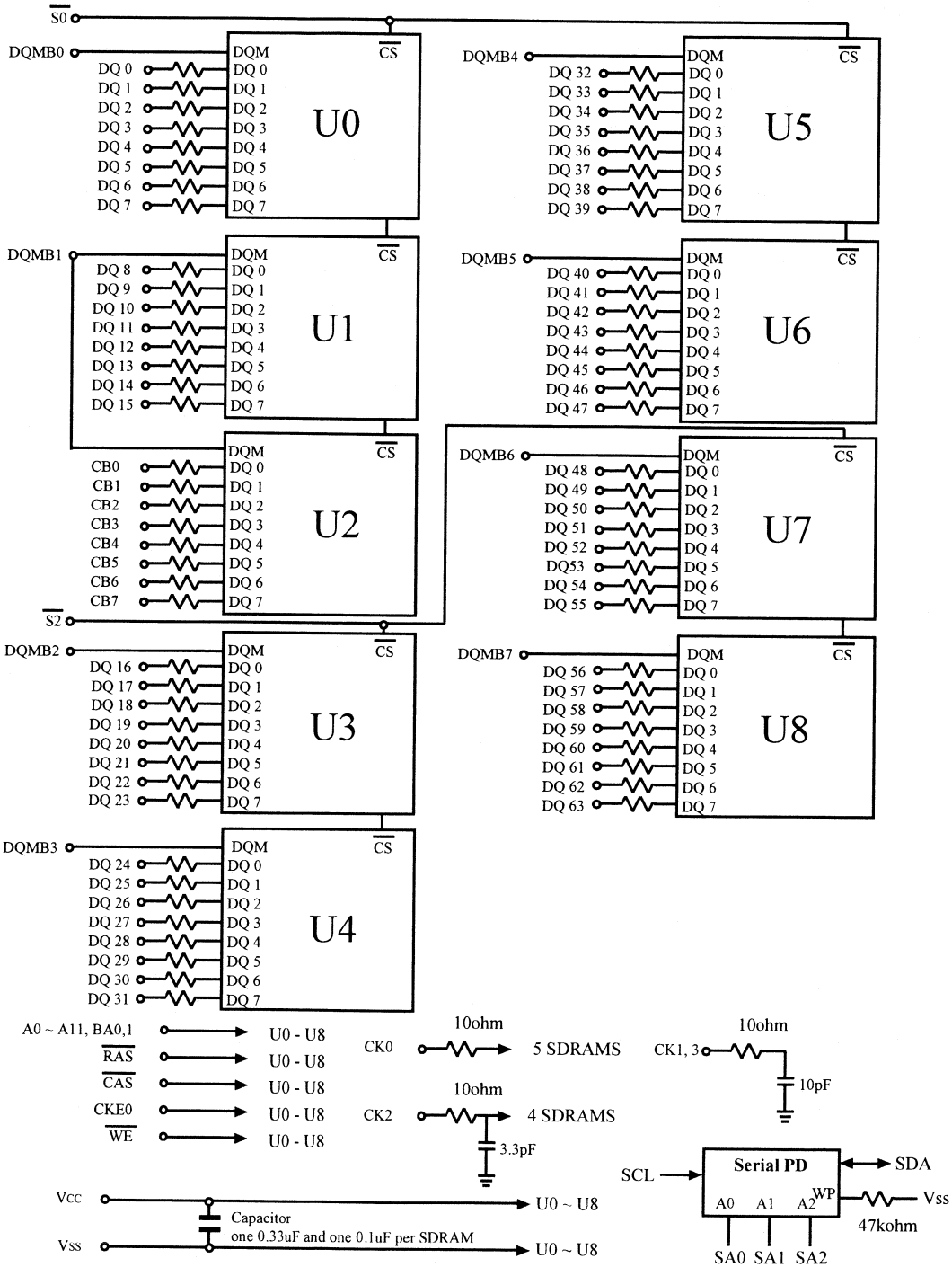
CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{*S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	*CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{*S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0, 2}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=7.0ns	70h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=50ns	32h	
31	Module Bank Density	64MBytes	10h	
32	Command & address signal input setup time	t_{AS} = 2ns	20h	
33	Command & address signal input hold time	t_{AH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
36~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		68h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM2739233CTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			39h	9
80			32h	2
81			33h	3
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			43h	C
84			54h	T
85			47h	G
86			2Dh	-
87			37h	7
88			4Ah	J
89			20h	
90			20h	
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		AFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to Vss.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, V_{SS}, V_{SSQ}= 0 V)
(GM72V66841CT)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	540	-	585	-	450	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	720	-	765	-	630	mA		
Standby current in power down		I_{CC2P}	-	27	-	27	-	27	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	18	-	18	-	18	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	180	-	180	-	180	mA	CKE,CS = V_{IL}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	81	-	81	-	81	mA	CKE = V_{IL}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	54	-	54	-	54	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	45	-	45	-	45	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	270	-	270	-	270	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	180	-	180	-	180	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	630	-	855	-	630	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	1080	-	1395	-	1080	mA		
Refresh current	(CL= 2)	I_{CC5}	-	720	-	765	-	540	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	1170	-	1260	-	990	mA		
Self refresh current		I_{CC6}	-	18	-	18	-	18	mA	V_{IH} ≥ V_{CC} - 0.2 V_{IL} ≤0.2V	7

Parameter	Symbol	-7		-8		-10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$, $\overline{S2}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB1)	-	TBD	pF	1, 2
C_{I6}	Input capacitance (DQMB0, 2, 3, 4, 5, 6, 7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, Vss, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

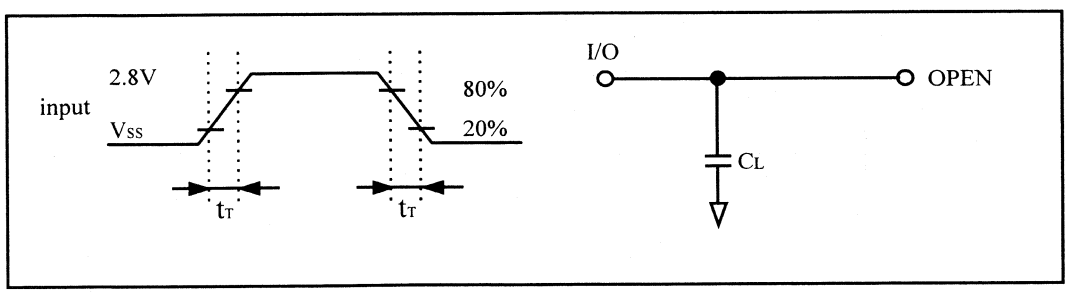
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter	Symbol	-7		-8		-10		Notes
Frequncy(MHz)		100	66	125	83	100	66	
t_{CK} (ns)		10	15	8	12	10	15	
Active command to column command (same bank)	l_{RCD}	3	2	3	2	3	2	1
Active command to active command period (same bank)	l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)	l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)	l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)	l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)	l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time	l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input	l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence (CL=2)	l_{HZP}	-	2	-	2	-	2	
Precharge command to high impedence (CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)	l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) (CL=2)	l_{EP}	-	- 1	-	- 1	-	- 1	
Last data out to precharge (early precharge) (CL=3)	l_{EP}	-2	- 2	-2	- 2	-2	- 2	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	

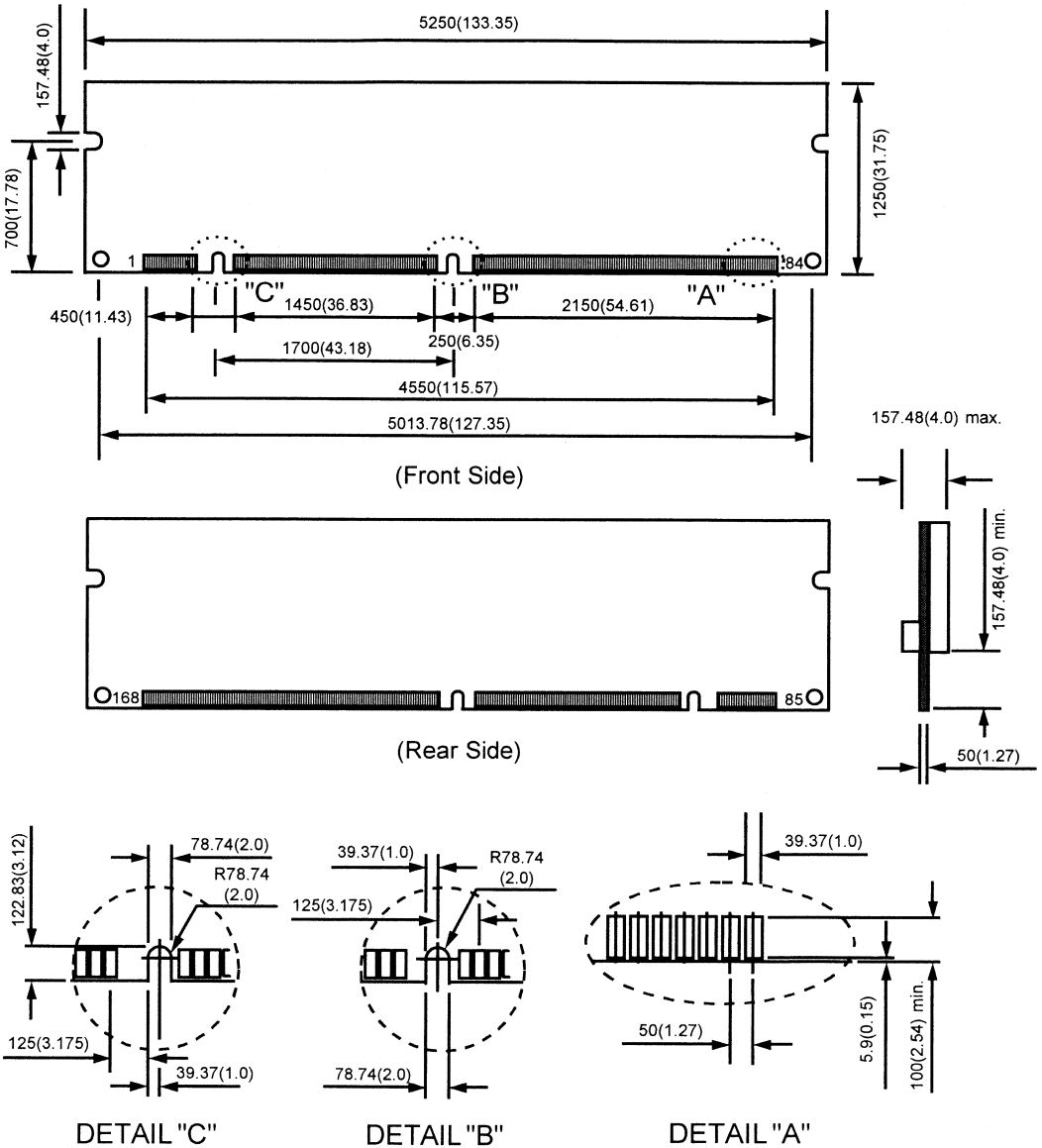
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	- 7		- 8		- 10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

LG Semicon Co.,Ltd.

GMM2739230CTG

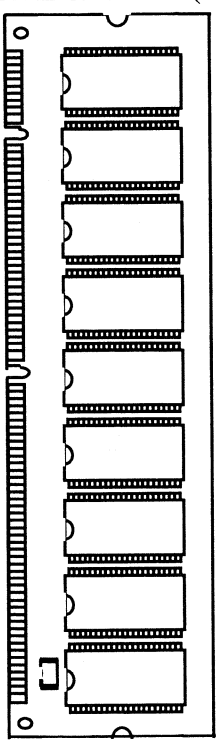
8,388,608 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM2739230CTG is a 8M x 72bits Synchronous Dynamic RAM MODULE which is assembled 9 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package, 2 pieces of 16 bits Register in 48 pin TSSOP package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM2739230CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2739230CTG provides common data inputs and outputs.

- **GMM2739230CTG** (Single Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
REGE	Register Enable
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
WP	Write Protect for SPD
DU	Don't Use

GMM26416233CNTG

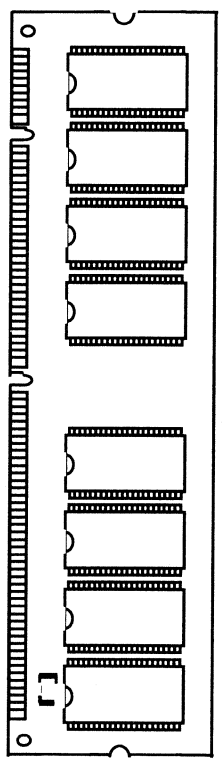
16,777,216 WORDS x64bit
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM26416233CNTG is a 16M x 64bits Synchronous Dynamic RAM MODULE which is assembled 16 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM26416233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM26416233CNTG provides common data inputs and outputs.

- **GMM26416233CNTG** (Double Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

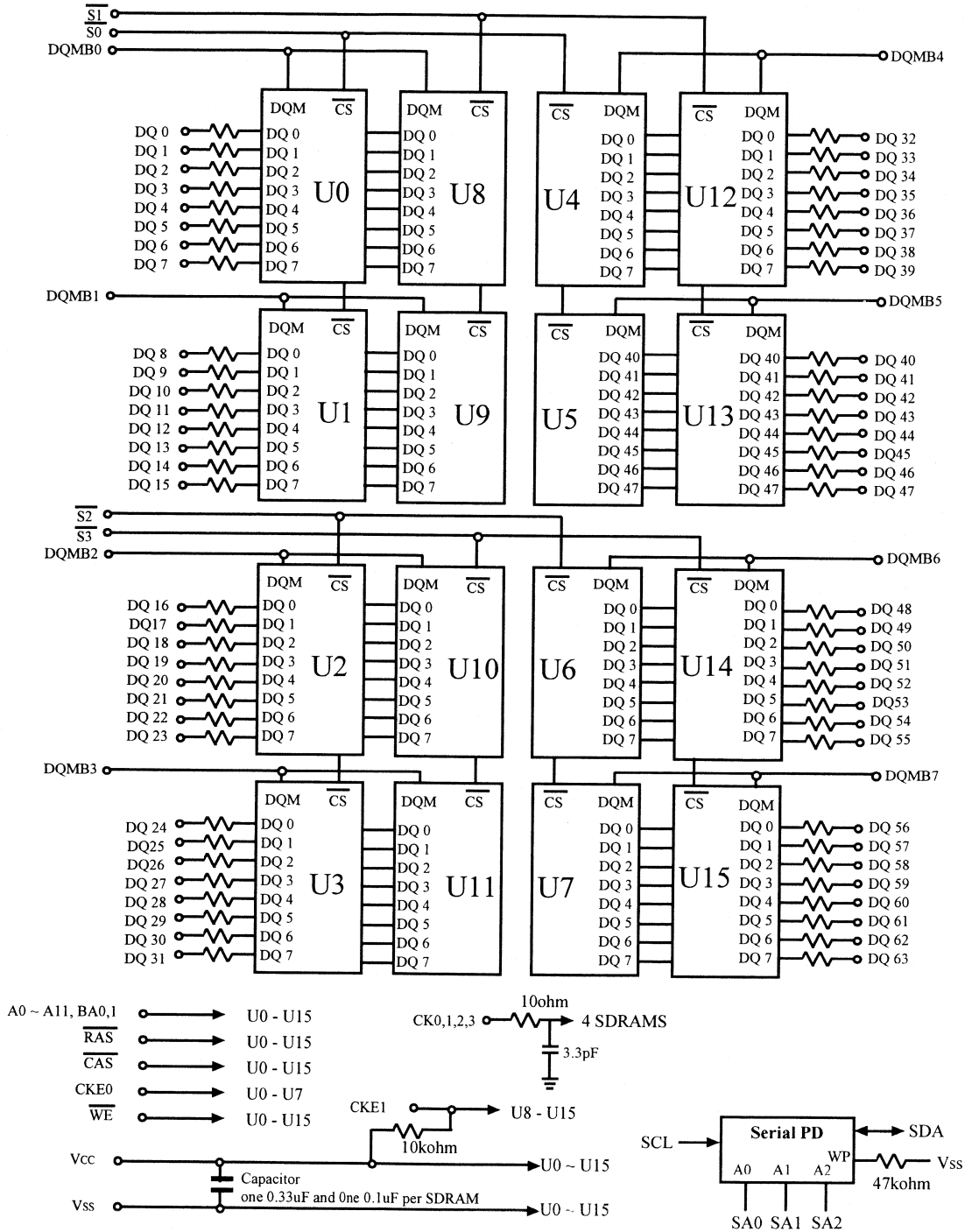
CK0, 1, 2, 3	Clock input
CKE0,1	Clock Enable
$\overline{S0,1,2,3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	WP	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0,1,2,3}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	64 bits	40h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	Non-Parity	00h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	N/A	00h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=7.0ns	70h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=50ns	32h	
31	Module Bank Density	64 MBytes	10h	
32	Command & address signal input setup time	t_{AS} = 2ns	20h	
33	Command & address signal input hold time	t_{AH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1.2	01h	
63	Checksum for bytes 0 ~ 62		57h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM26416233CNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			36h	6
78			34h	4
79			31h	1
80			36h	6
81			32h	2
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			33h	3
84			43h	C
85			4Dh	N
86			54h	T
87			47h	G
88			2Dh	-
89			37h	7
90			4Ah	J
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to Vss

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, V_{SS}, V_{SSQ}= 0 V)
(GM72V66841CT)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	640	-	680	-	560	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	800	-	840	-	720	mA		
Standby current in power down		I_{CC2P}	-	48	-	48	-	48	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	32	-	32	-	32	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	320	-	320	-	320	mA	CKE,CS = V_{IL}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	144	-	144	-	144	mA	CKE = V_{IL}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	96	-	96	-	96	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	80	-	80	-	80	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	480	-	480	-	480	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	320	-	320	-	320	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	720	-	920	-	720	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	1120	-	1400	-	1120	mA		
Refresh current	(CL= 2)	I_{CC5}	-	800	-	840	-	640	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	1200	-	1280	-	1040	mA		
Self refresh current		I_{CC6}	-	176	-	176	-	176	mA	$V_{IH} \geq V_{CC}$ - 0.2 $V_{IL} \leq$ 0.2V	7

Parameter	Symbol	- 7		- 8		- 10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq Vout \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

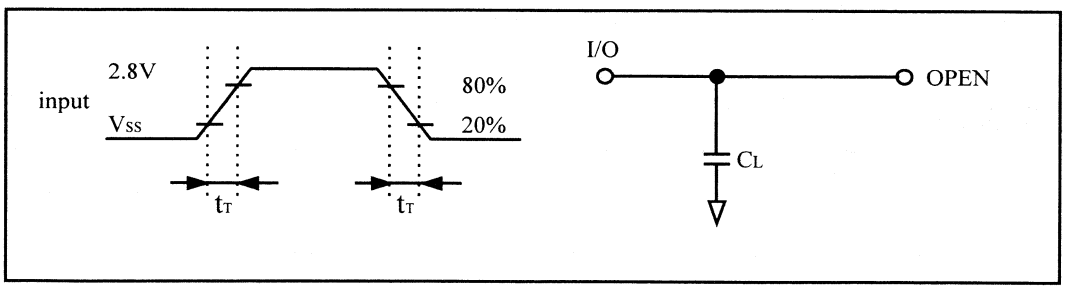
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

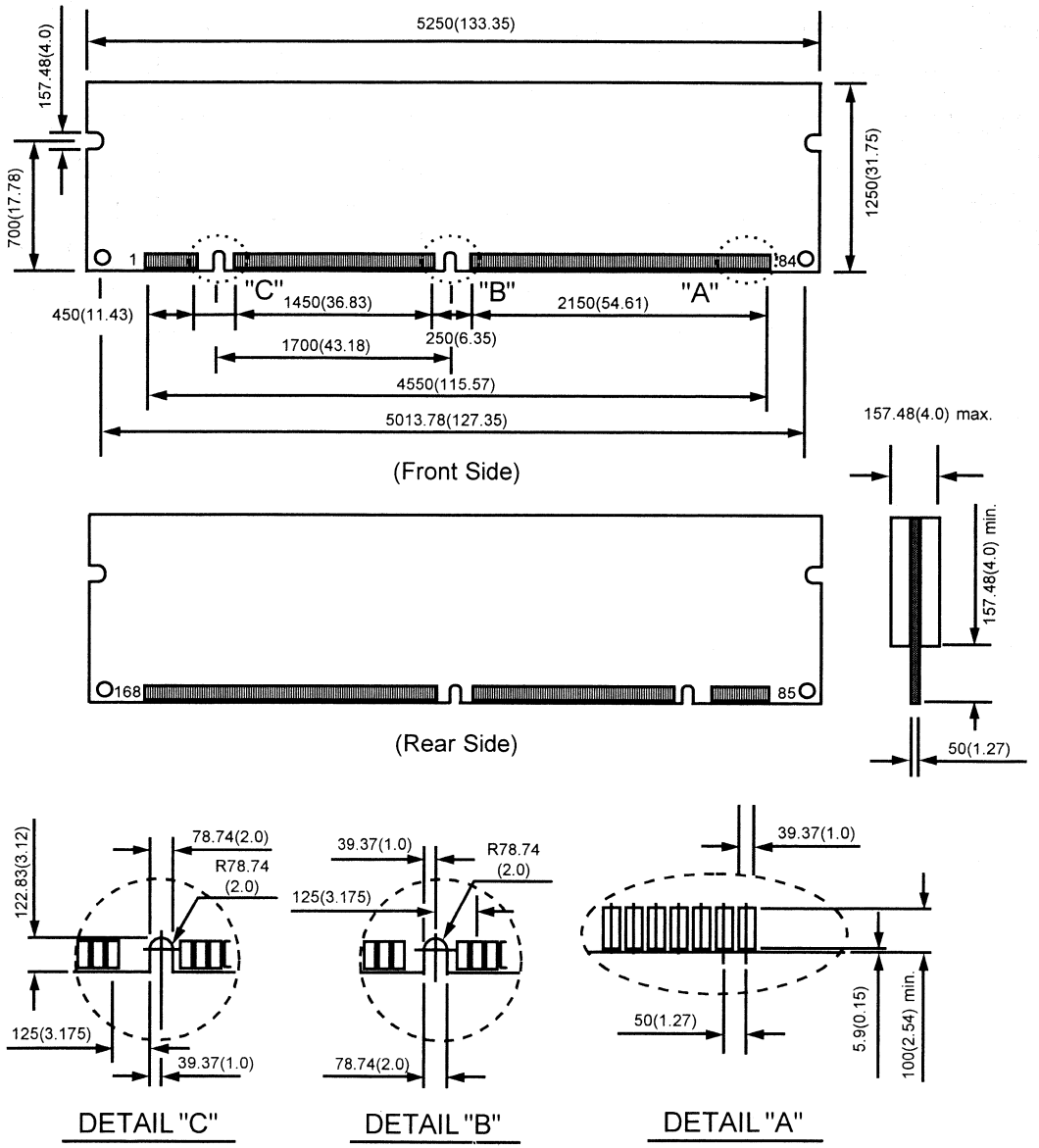
Parameter	Symbol	-7		-8		-10		Notes
Frequncy(MHz)		100	66	125	83	100	66	
t_{CK} (ns)		10	15	8	12	10	15	
Active command to column command (same bank)	l_{RCD}	3	2	3	2	3	2	1
Active command to active command period (same bank)	l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)	l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)	l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)	l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)	l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time	l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input	l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence (CL=2)	l_{HZP}	-	2	-	2	-	2	
Precharge command to high impedence (CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)	l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) (CL=2)	l_{EP}	-	-1	-	-1	-	-1	
Last data out to precharge (early precharge) (CL=3)	l_{EP}	-2	-2	-2	-2	-2	-2	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ±5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

GMM27316233CNTG

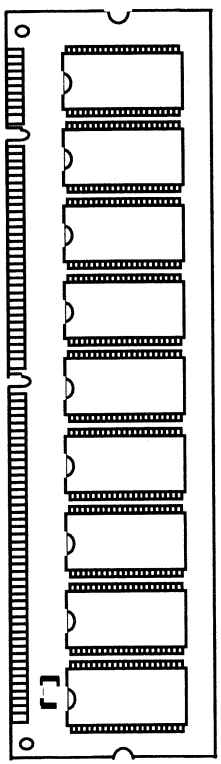
16,777,216 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM27316233CNTG is a 16M x 72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 8M x 8bits Synchronous DRAMs in 54 pin TSOP II package and one 2048 bit EEPROM in 8pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM27316233CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM27316233CNTG provides common data inputs and outputs.

- **GMM27316233CNTG** (Double Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

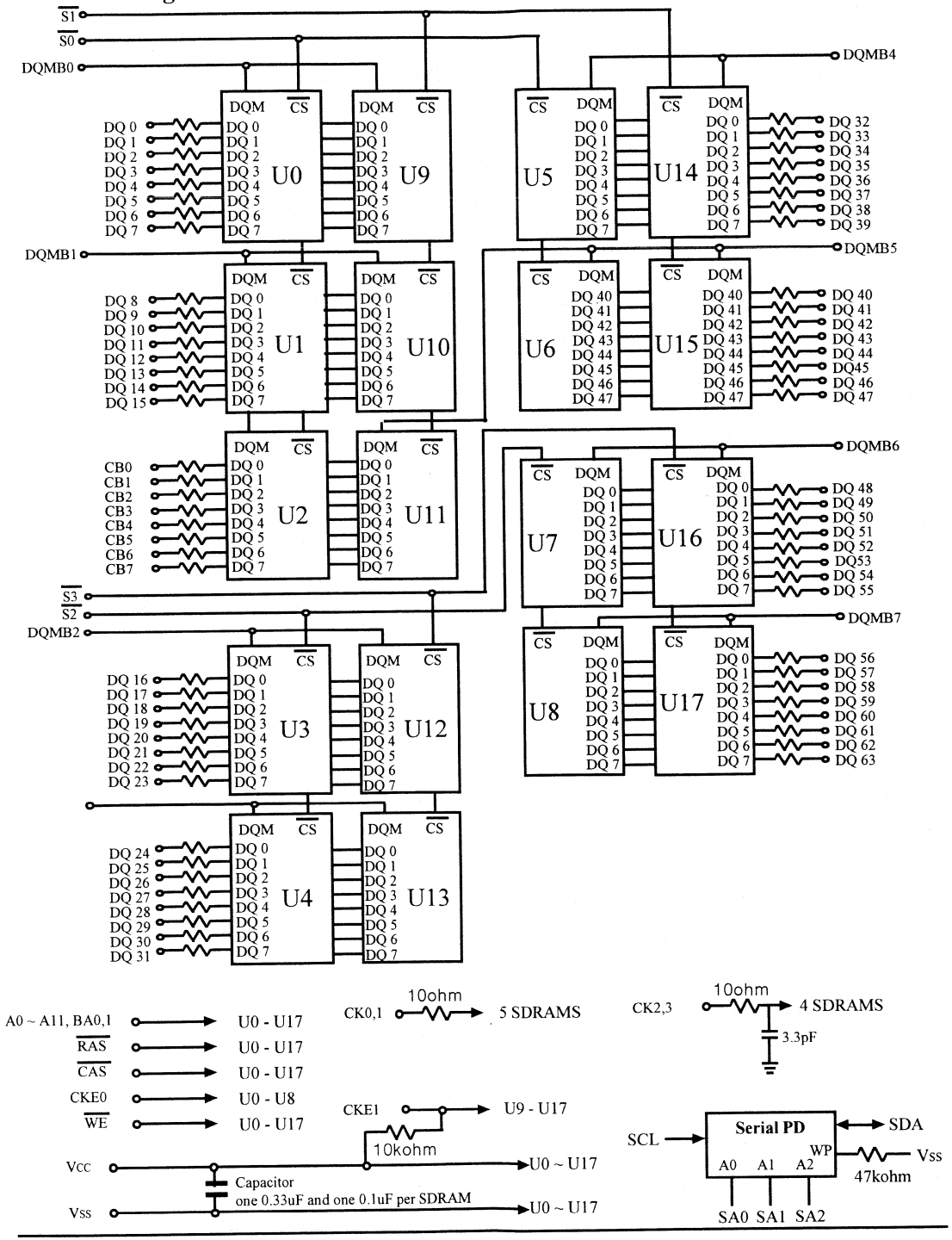
CK0, 1, 2, 3	Clock input
CKE0,1	Clock Enable
$\overline{S0,1,2,3}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	29	DQMB1	57	DQ18	85	Vss	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	Vcc	87	DQ33	115	$\overline{RAS}$	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	*VREF, NC	90	Vcc	118	A3	146	*VREF, NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	*A12	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	Vcc	101	DQ45	129	$\overline{S3}$	157	Vcc
18	Vcc	46	DQMB2	74	DQ28	102	Vcc	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	CB0	49	Vcc	77	DQ31	105	CB4	133	Vcc	161	DQ63
22	CB1	50	NC	78	Vss	106	CB5	134	NC	162	Vss
23	Vss	51	NC	79	CK2	107	Vss	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	Vcc	112	DQMB4	140	DQ49	168	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0, 1, 2, 3 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0,1 (input pin)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S}$0,1,2,3 (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A11 (input pins)	Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0,1 (input pin)	BA0,1 are bank select signal. If BA0 is Low and BA1 is High, bank 0 is selected. If BA0 is High and BA1 is Low, bank 1 is selected. If BA0 is Low and BA1 is High, bank 2 is selected. If BA0 is High and BA1 is High, bank 3 is selected.
DQ0 ~ DQ63 CB0 ~ CB7 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	12	0Ch	
4	# of column addresses on this assembly	9	09h	
5	# of module banks on this assembly	2 banks	02h	
6	Data width of this assembly	72 bits	48h	
7	Data width continuation.	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	t_{CK3}=10ns	A0h	100MHz
10	SDRAM access time from clock	t_{AC3}=6.0ns	60h	
11	DIMM configuration type	ECC	02h	
12	Refresh rate/type	4096/64ms : Normal	80h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	x8	08h	
15	Minimum clock delay, Back to Back Random Column Address	1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	
17	# of banks on each SDRAM device	4 banks	04h	
18	CAS # Latency	1, 2 & 3	07h	
19	$\overline{CS}$ # Latency	0	01h	
20	Write Latency	0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	
22	SDRAM device attributes : General		0Fh	
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	

Byte No.	Function description	Function support	Hex Value	Value
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=7.0ns	70h	
25	Minimum Clock Cycle Time at CL X-2	N/A	00h	
26	Maximum Data Access Time from Clock @CL X-2	N/A	00h	
27	Minimum Row Precharge Time	t_{RP}=20ns	14h	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=20ns	14h	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=50ns	32h	
31	Module Bank Density	64MBytes	10h	
32	Command & address signal input setup time	t_{AS} = 2ns	20h	
33	Command & address signal input hold time	t_{AH} = 1ns	10h	
34	Data signal input setup time	t_{DS} = 2ns	20h	
35	Data signal input hold time	t_{DH} = 1ns	10h	
36~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev. 1.2	01h	
63	Checksum for bytes 0 ~ 62		69h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturing location	Korea	52h	
73	Manufacturer Part Number	GMM27316233CNTG-7J	47h	G
74	= Allowed characters include 0-9, A-Z=		4Dh	M
75			4Dh	M
76			32h	2
77			37h	7
78			33h	3
79			31h	1
80			36h	6
81			32h	2
82			33h	3

Byte No.	Function description	Function support	Hex Value	Note
83			33h	3
84			43h	C
85			4Dh	N
86			54h	T
87			47h	G
88			2Dh	-
89			37h	7
90			4Ah	J
91~92	Revision Code	Initial release	00h	Rev.0
93	Date Code	WW	32h	50 week
94		YY	60h	96 year
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Serial data	N/A	00h	
126	Intel Specification for frequency	100MHz	64h	
127	Intel specification details for 100Mhz support		FFh	
128~135	System Integrator & ID		00h	
136~150	System Integrator's P/N		00h	
151~152	System Integrator's D/C		00h	
153~165	System Integrator's P/N		00h	
166	Checksum for bytes 128~ 165		00h	
167~189	Top level system serial no.		00h	
190~221	Open		00h	
222	Checksum for bytes 167~221		00h	
223~253	Open		00h	
254	Checksum for Bytes 223 ~ 253		00h	
255	Checksum for bytes 0 ~ 128		00h	

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to Vss	V_T	-0.5 to Vcc+0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to Vss	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_T	1.0	W	
Operating temperature	Topr	0 to +70	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 70℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	Vcc + 0.3	V	1, 2 , 3
Input low voltage	V_{IL}	-0.3	0.8	V	1, 4

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = Vcc + 0.5V for pulse width $\leq$ 5ns at Vcc.(DQ pins).

3. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

4. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ±0.3 V, V_{SS}, V_{SSQ}= 0 V)
(GM72V66841CT)

Parameter		Symbol	-7		-8		-10		Unit	Test conditions	Notes
			Min	Max	Min	Max	Min	Max			
Operating current	(CL= 2)	I_{CC1}	-	720	-	765	-	630	mA	Burst length= 1 t_{RC} = min	1, 2, 3
	(CL= 3)	I_{CC1}	-	900	-	945	-	810	mA		
Standby current in power down		I_{CC2P}	-	54	-	54	-	54	mA	CKE = V_{IL}, t_{CK} = 12 ns	5
Standby current in power down (input signal stable)		I_{CC2PS}	-	36	-	36	-	36	mA	CKE=V_{IL}, t_{CK}= ∞	6
Standby current in non power down ($\overline{CAS}$ latency=2)		I_{CC2N}	-	360	-	360	-	360	mA	CKE,CS = V_{IL}, t_{CK} = 12ns	4
Standby current in non power down (input signal stable)		I_{CC2NS}	-	162	-	162	-	162	mA	CKE = V_{IL}, t_{CK} = ∞	8
Active standby current in power down		I_{CC3P}	-	108	-	108	-	108	mA	CKE = V_{IL}, t_{CK} = 12 ns, DQ = High-Z	1,2,5
Active standby current in power down (input signal stable)		I_{CC3PS}	-	90	-	90	-	90	mA	CKE = V_{IL}, t_{CK} = ∞	2,6
Active standby current in non power down		I_{CC3N}	-	540	-	540	-	540	mA	CKE,CS = V_{IH}, t_{CK} = 12 ns, DQ = High-Z	1,2,4
Active standby current in non power down (input signal stable)		I_{CC3NS}	-	360	-	360	-	360	mA	CKE = V_{IH}, t_{CK} = ∞	2,8
Burst operating current	(CL= 2)	I_{CC4}	-	810	-	1035	-	810	mA	t_{CK} = min BL = 4	1,2,3
	(CL= 3)	I_{CC4}	-	1260	-	1575	-	1260	mA		
Refresh current	(CL= 2)	I_{CC5}	-	900	-	945	-	720	mA	t_{RC} = min	3
	(CL= 3)	I_{CC5}	-	1350	-	1440	-	1170	mA		
Self refresh current		I_{CC6}	-	198	-	198	-	198	mA	$V_{IH} \geq V_{CC}$ - 0.2 $V_{IL} \leq$0.2V	7

Parameter	Symbol	- 7		- 8		- 10		Unit	Test conditions	Notes
		Min	Max	Min	Max	Min	Max			
Input leakage current	I_{LI}	-10	10	-10	10	-10	10	μA	$0 \leq V_{in} \leq V_{CC}$	
Output leakage current	I_{LO}	-10	10	-10	10	-10	10	μA	$0 \leq V_{out} \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	-	2.4	-	2.4	-	V	I_{OH} = -2 mA	
Output low voltage	V_{OL}	-	0.4	-	0.4	-	0.4	V	I_{OL} =2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Addresses are changed once per one cycle.
4. Addresses are changed once per two cycles.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.
8. Input signals are V_{IH} or V_{IL} fixed.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	TBD	pF	1, 2
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	TBD	pF	1, 2
C_{I3}	Input capacitance (CK0, CK1, CK2, CK3)	-	TBD	pF	1, 2
C_{I4}	Input capacitance ($\overline{S0}$ ~ $\overline{S3}$)	-	TBD	pF	1, 2
C_{I5}	Input capacitance (DQMB1, DQMB5)	-	TBD	pF	1, 2
C_{I6}	Input capacitance (DQMB0, 2, 3, 4, 6, 7)	-	TBD	pF	1, 2
$C_{I/O}$	I/O capacitance (DQ0 ~ 63, CB0 ~ 7)	-	TBD	pF	1, 2

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V)

Parameter		Symbol	-7		-8		-10		Unit	Notes
			Min	Max	Min	Max	Min	Max		
System clock cycle time	(CL=2)	t_{CK}	15	-	12	-	15	-	ns	1
	(CL=3)	t_{CK}	10	-	8	-	10	-		
CLK high pulse width		t_{CKH}	3	-	3	-	3	-	ns	1
CLK low pulse width		t_{CKL}	3	-	3	-	3	-	ns	1
Access time from CLK	(CL=2)	t_{AC}	-	7	-	8	-	9	ns	1, 2
	(CL=3)	t_{AC}	-	6	-	6	-	8		
Data-out hold time		t_{OH}	2.5	-	2.5	-	2.5	-	ns	1, 2
CLK to Data-out low impedence		t_{LZ}	2	-	2	-	2	-	ns	1, 2, 3
CLK to Data-out high impedence (CL = 2,3)		t_{HZ}	-	6	-	6	-	7	ns	1, 4
Data-in setup time		t_{DS}	2	-	2	-	2	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	2	-	2	-	ns	1
Address hold time		t_{AH}	1	-	1	-	1	-	ns	1
CKE setup time		t_{CES}	2	-	2	-	2	-	ns	1, 5
CKE setup time for power down exit		t_{CESP}	2	-	2	-	2	-	ns	1
CKE hold time		t_{CEH}	1	-	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time		t_{CS}	2	-	2	-	2	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time		t_{CH}	1	-	1	-	1	-	ns	1
Ref/Active to Ref/Active command period		t_{RC}	70	-	72	-	90	-	ns	1
Active to Precharge command period		t_{RAS}	50	120000	48	120000	60	120000	ns	1
Active command to column command (same bank)		t_{RCD}	20	-	24	-	30	-	ns	1
Precharge to active command period		t_{RP}	20	-	24	-	30	-	ns	1

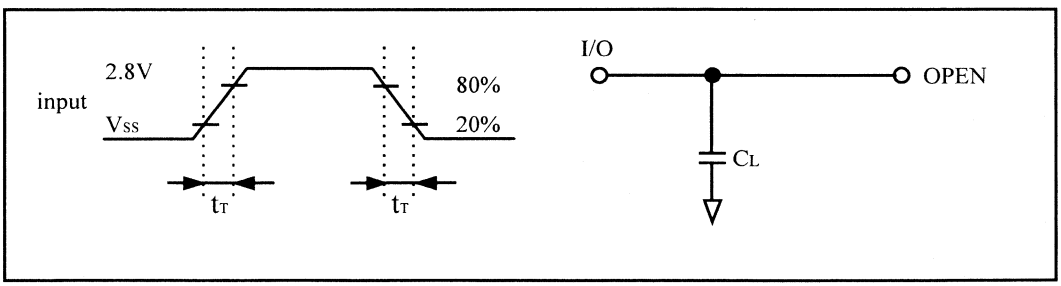
AC Characteristics (Ta = 0 to 70℃, V_{CC}, V_{CCQ} = 3.3 V ± 0.3 V, V_{SS}, V_{SSQ} = 0 V) (Continued)

Parameter	Symbol	-7		-8		-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write recovery or data-in to precharge lead time	t_{RWL}	10	-	10	-	15	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	16	-	20	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.
2. Access time is measured at 1.40V. Load condition is C_L = 50pF without termination.
3. t_{LZ} (max)defines the time at which the outputs achieves the low impedence state.
4. t_{HZ} (max)defines the time at which the outputs achieves the high impedence state.
5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency

Parameter	Symbol	-7		-8		-10		Notes
Frequncy(MHz)		100	66	125	83	100	66	
t_{CK} (ns)		10	15	8	12	10	15	
Active command to column command (same bank)	l_{RCD}	3	2	3	2	3	2	1
Active command to active command period (same bank)	l_{RC}	7	6	9	6	9	6	= [l_{RAS} +l_{RP}], 1
Active command to precharge command (same bank)	l_{RAS}	5	4	6	4	6	4	1
Precharge command to active command (same bank)	l_{RP}	2	2	3	2	3	2	1
Write recovery or data-in to precharge command (same bank)	l_{RWL}	1	1	1	1	1	1	1
Active command to active command (different bank)	l_{RRD}	2	2	2	2	2	2	1
Self refresh exit time	l_{SREX}	2	2	2	2	2	2	2
Last data in to active command (Auto precharge, same bank)	l_{APW}	5	3	5	3	5	3	= [l_{RWL} +l_{RP}], 1
Self refresh exit to command input	l_{SEC}	9	6	9	6	9	6	= [l_{RC}]
Precharge command to high impedence (CL=2)	l_{HZP}	-	2	-	2	-	2	
Precharge command to high impedence (CL=3)	l_{HZP}	3	3	3	3	3	3	
Last data out to active command (auto precharge) (same bank)	l_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge) (CL=2)	l_{EP}	-	- 1	-	- 1	-	- 1	
Last data out to precharge (early precharge) (CL=3)	l_{EP}	-2	- 2	-2	- 2	-2	- 2	
Column command to column command	l_{CCD}	1	1	1	1	1	1	
Write command to data in latency	l_{WCD}	0	0	0	0	0	0	
DQM to data in	l_{DID}	0	0	0	0	0	0	
DQM to data out	l_{DOD}	2	2	2	2	2	2	
CKE to CLK disable	l_{CLE}	1	1	1	1	1	1	
Register set to active command	l_{RSA}	1	1	1	1	1	1	
$\overline{CS}$ to command disable	l_{CDD}	0	0	0	0	0	0	
Power down exit to command input	l_{PEC}	1	1	1	1	1	1	

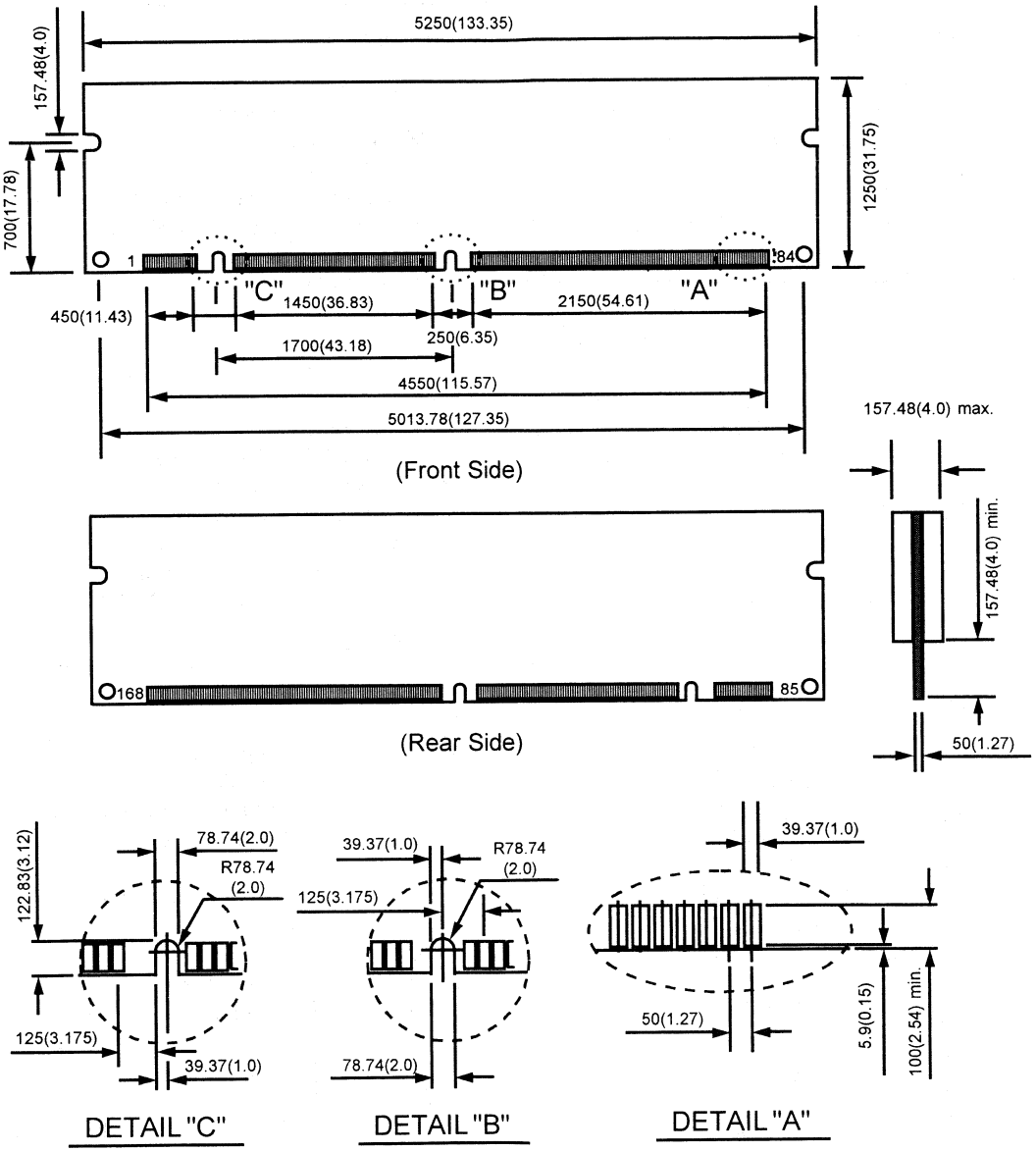
Relationship Between Frequency and Minimum Latency

Parameter		Symbol	-7		-8		-10		Notes
Frequncy(MHz)			100	66	125	83	100	66	
t_{CK} (ns)			10	15	8	12	10	15	
Burst stop to output valid data hold	(CL=2)	l_{BSR}	-	1	-	1	-	1	
	(CL=3)	l_{BSR}	2	2	2	2	2	2	
Burst stop to output high impedence	(CL=2)	l_{BSH}	-	2	-	2	-	2	
	(CL=3)	l_{BSH}	3	3	3	3	3	3	
Burst stop to write data ignore		l_{BSW}	0	0	0	0	0	0	

Notes : 1. l_{RCD} to l_{RRD} are recommended value.
2. 2 clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mil (mm)
* (1 mil = 1/1000 inches)



NOTE : 1. Tolerances on all dimensions ± 5 (0.127) unless otherwise specified.
2. Thickness includes Plating and / or Metallization.

LG Semicon Co.,Ltd.

GMM27316230CTG

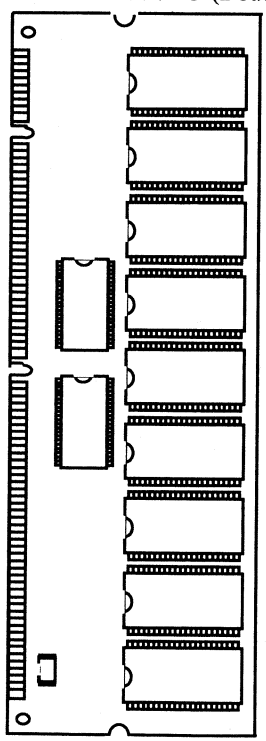
16,777,216 WORDS x72BIT
SYNCHRONOUS DYNAMIC RAM MODULE

Description

The GMM27316230CTG is a 16M x 72bits Synchronous Dynamic RAM MODULE which is assembled 18 pieces of 16M x 4bits Synchronous DRAMs in 54 pin TSOP II package, 2 pieces of 16 bits Register in 48 pin TSSOP package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 168 pin printed circuit board with decoupling capacitors. The GMM27316230CTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM27316230CTG provides common data inputs and outputs.

- **GMM27316230CTG** (Double Side)



Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

Pin Name

CK0, 1, 2, 3	Clock input
$\overline{CKE0}$	Clock Enable
$\overline{S0, 2}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0 ~ A11	Address input
BA0,1	Bank Address input
REGE	Register Enable
DQ0 ~ 63	Data input / output
CB0 ~ 7	Check Bits
DQMB0 ~ 7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input/ output
SCL	Serial Clock
SA0 ~ 2	Address in EEPROM
WP	Write Protect for SPD
DU	Don't Use

GMM2642227CNTG

2,097,512 WORDS x 64 BIT
SYNCHRONOUS DYNAMIC RAM SO-DIMM

Description

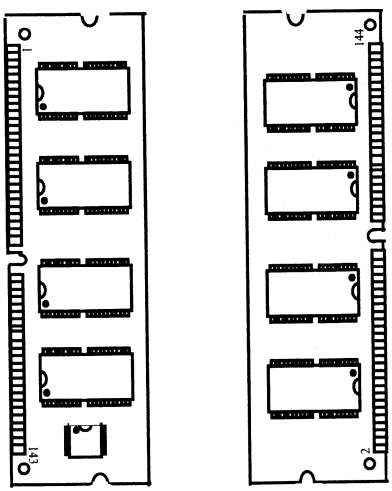
The GMM2642227CNTG is a 2M x 64 bits Synchronous Dynamic RAM SO-DIMM which is assembled 8 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 144 pin printed circuit board with decoupling capacitors. The GMM2642227CNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2642227CNTG provides common data inputs and outputs.

Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

- **GMM2642227CNTG** (Both Side)



Pin Name

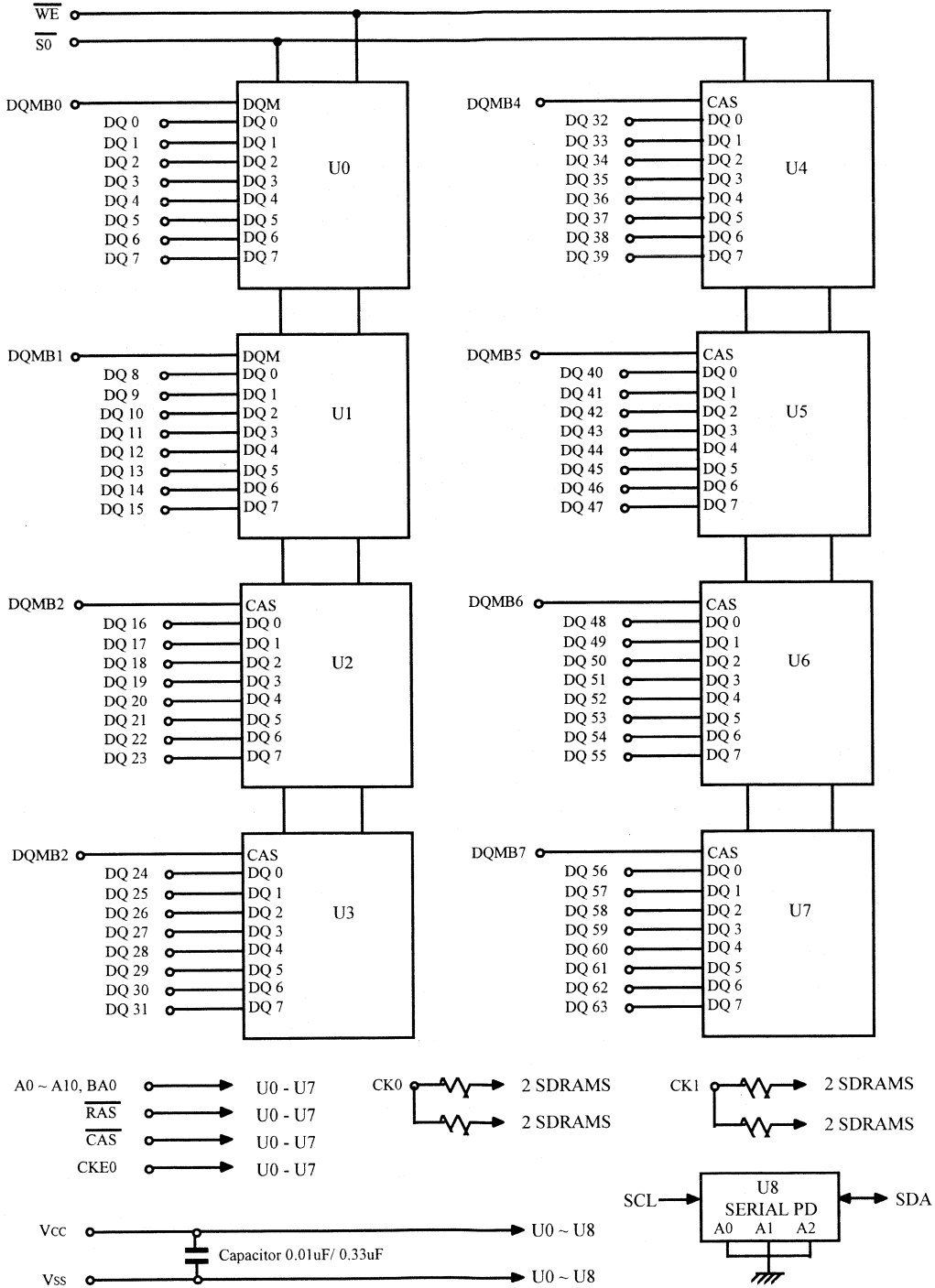
CK0,1	Clock inputs
CKE0	Clock Enable
$\overline{S0}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
BA0	Bank Address input
DQ0~63	Data input / output
DQMB0~7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	25	DQMB1	49	DQ13	73	NU	97	DQ22	121	DQ24
2	Vss	26	DQMB5	50	DQ45	74	CK1	98	DQ54	122	DQ56
3	DQ0	27	Vcc	51	DQ14	75	Vss	99	DQ23	123	DQ25
4	DQ32	28	Vcc	52	DQ46	76	Vss	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	Vcc	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	Vcc	126	DQ58
7	DQ2	31	A1	55	Vss	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	Vss	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	Vcc	105	A8	129	Vcc
10	DQ35	34	A5	58	NC	82	Vcc	106	BA0	130	Vcc
11	VDD	35	Vss	59	NC	83	DQ16	107	Vss	131	DQ28
12	VDD	36	Vss	60	NC	84	DQ48	108	Vss	132	DQ60
13	DQ4	37	DQ8	61	CK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1*	134	DQ61
15	DQ5	39	DQ9	63	Vcc	87	DQ18	111	A10/AP	135	DQ30
16	DQ37	40	DQ41	64	Vcc	88	DQ50	112	A11*	136	DQ62
17	DQ5	41	DQ10	65	$\overline{RAS}$	89	DQ19	113	Vcc	137	DQ31
18	DQ38	42	DQ42	66	CAS	90	DQ51	114	Vcc	138	DQ63
19	DQ7	43	DQ11	67	$\overline{WE}$	91	Vss	115	DQMB2	139	Vss
20	DQ39	44	DQ43	68	CKE1*	92	Vss	116	DQMB6	140	Vss
21	Vss	45	Vcc	69	$\overline{S0}$	93	DQ20	117	DQMB3	141	SDA
22	Vss	46	Vcc	70	A12	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	S1	95	DQ21	119	Vss	143	Vcc
24	DQMB4	48	DQ44	72	A13	96	DQ53	120	Vss	144	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0,1 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes(2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	1
4	# of column addresses on this assembly	9	09h	2
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly(Continued)	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	00h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	t_{CCD} = 1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	# of banks on each SDRAM device	2 banks	02h	
18	$\overline{CAS}$ Latency	$\overline{CAS}$ Latency = 1, 2 & 3	07h	7
19	$\overline{CS}$ Latency	$\overline{CS}$ latency = 0	01h	
20	Write Latency	Write latency = 0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	

Byte No.	Function description	Function support	Hex Value	Note
22	SDRAM device attributes : General		0Fh	5
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9.5ns	95h	
		t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		A3h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation Code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturer location	Korea	52h	
73	Manufacturer 's part number	G (GMM2642227CNTG-10K/J)	47h	
74	Allowed characters 0-9, a-z and space	M	4Dh	
75		M	4Dh	
76		2	32h	
77		6	36h	
78		4	34h	
79		2	32h	
80		2	32h	
81		2	32h	
82		7	37h	

Byte No.	Function description	Function support	Hex Value	Note
83		B	42h	
84		N	4Eh	
85		T	54h	
86		G	47h	
87		-	2Dh	
88		1	31h	
89		0	30h	
90		K	4Bh	
91~92	Revision Code	Initial release (Rev.0)	00h	
93	Date Code	WW	00h	
94		YY	00h	
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Specific Data	N/A	00h	
126	Intel specfication CAS# Latency Support	66MHz	66h	
127	Manufacturing Date		06h	
128~255	Reserved		00h	

- Above data are based on the SPD specification of JEDEC standard and can be changed.

- Note : 1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
  2. If the bank select address of CA11 is excluded, this byte must be programmed by 0Ah
  3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
  So, the value of A0h is based on the minimum cycle time @ $\overline{CAS}$ latency = 3.
  In case of - 12 part, the minimum cycle time is 12ns, 18ns and 36ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
  So, the value of C0h is based on the minimum cycle time @ $\overline{CAS}$ latency = 3.

4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 75h is based on the access time @ $\overline{CAS}$ latency = 3.
   In case of - 12 part, the access time is 9ns, 12ns and 32ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @ $\overline{CAS}$ latency = 3.
5. LGS' SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supports, this byte must be programmed by 06h.
6. LGS' SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supports, this byte must be programmed by 05h.
7. LGS' SDRAM supports $\overline{CAS}$ latency of 1, 2 and 3. If $\overline{CAS}$ latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	8	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter		Symbol	-10		-12		Unit	Test conditions	Notes
			Min	Max	Min	Max			
Operating current		I_{CC1}	-	800	-	680	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)		I_{CC2}	-	24	-	24	mA	CKE=V_{IL}, t_{CK}=min	5
			-	16	-	16	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
			-	240	-	200	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)		I_{CC3}	-	56	-	56	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
			-	280	-	240	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current	(CL=2)	I_{CC4}	-	800	-	680	mA	t_{CK}=min BL = 4	1, 2, 4
	(CL=3)	I_{CC4}	-	1200	-	1000	mA		
Auto Refresh current		I_{CC5}	-	680	-	560	mA	t_{RC}=min	
Self refresh current		I_{CC6}	-	16	-	16	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V≤ V_{IL} ≤0.2V	7
Input leakage current		I_{LI}	-10	10	-10	10	μA	0≤Vin≤V_{CC}	
Output leakage current		I_{LO}	-10	10	-10	10	μA	0≤Vout≤V_{CC} I/O = disable	
Output high voltage		V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH}=-2mA	
Output low voltage		V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	50	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	45	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK1)	-	45	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$)	-	45	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	15	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	15	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	- 10		- 12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9.5	-	12		
	(CL=3)	t_{AC}	-	8	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

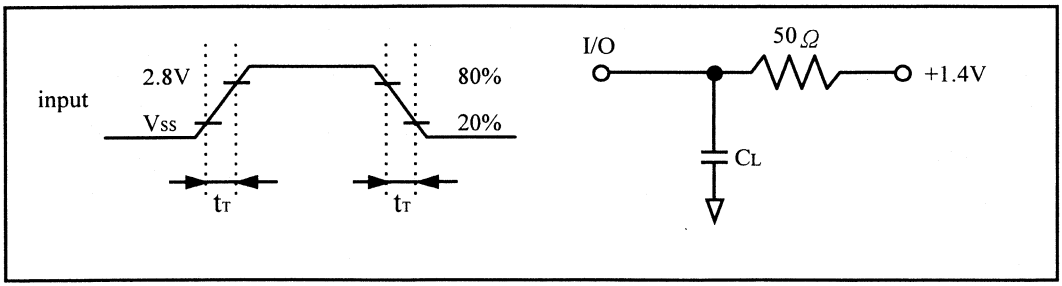
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	-10			-12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

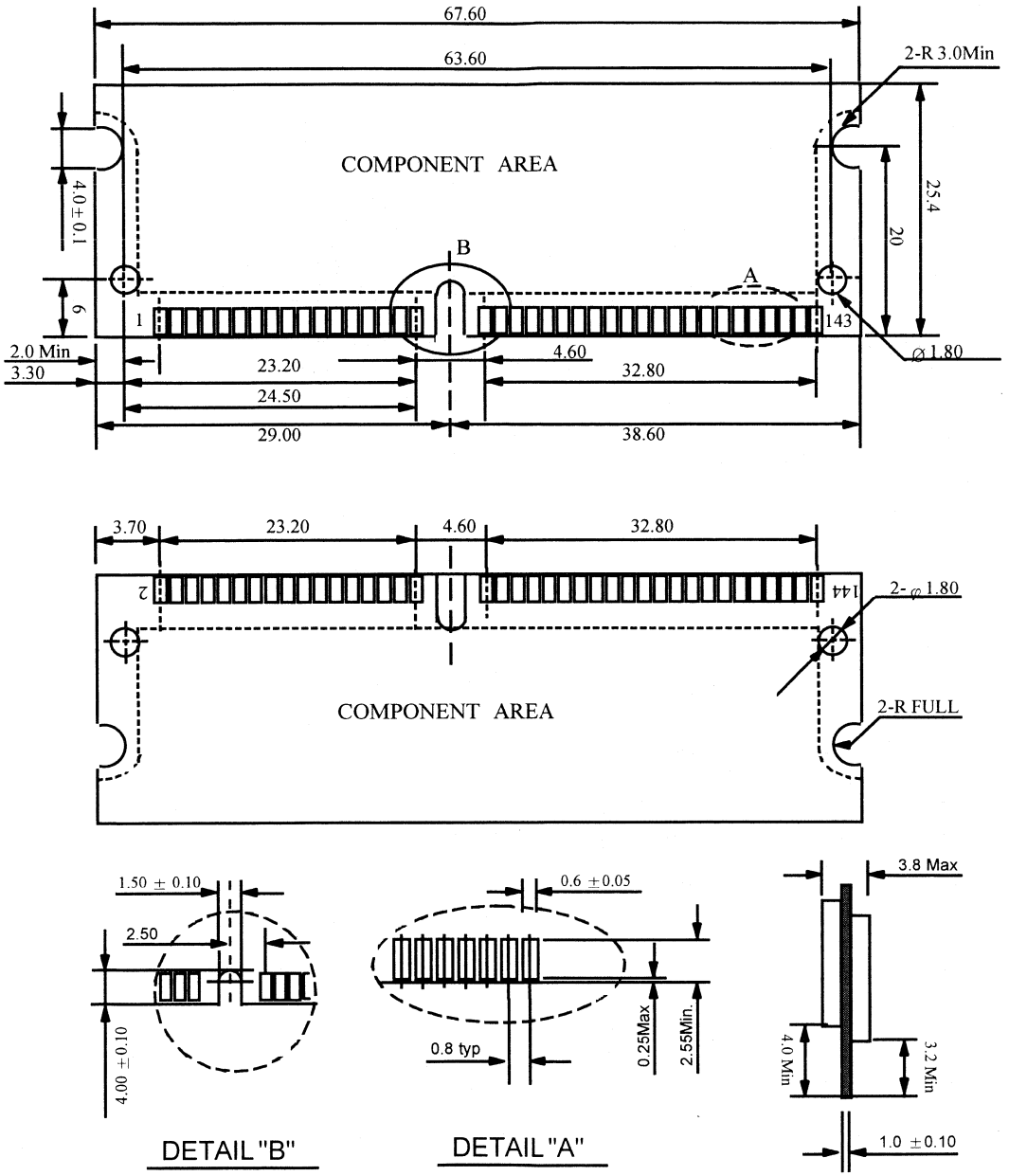
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

Package Dimension

Unit: mm



NOTE : 1. Tolerances on all dimensions ±0.15 unless otherwise specified.
2. Thickness(* Mark) includes Plating and / or Metallization.

LG Semicon Co.,Ltd.

GMM2642227DNTG

2,097,512 WORDS x 64 BIT
SYNCHRONOUS DYNAMIC RAM SO-DIMM

Description

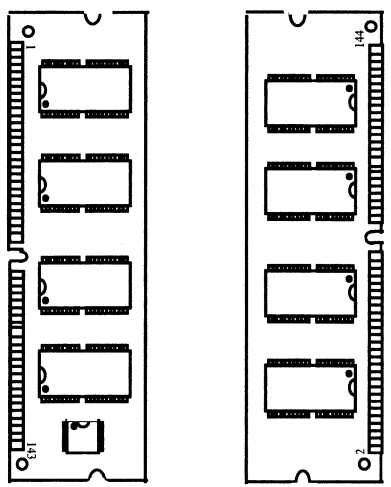
The GMM2642227DNTG is a 2M x 64 bits Synchronous Dynamic RAM SO-DIMM which is assembled 8 pieces of 2M x 8bits Synchronous DRAMs in 44 pin TSOP II package and one 2048 bit EEPROM in 8 pin TSSOP package mounted on a 144 pin printed circuit board with decoupling capacitors. The GMM2642227DNTG is optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size.

The GMM2642227DNTG provides common data inputs and outputs.

Features

- 3.3V ± 0.3V Power supply
- Maximum Clock frequency
  66 / 83 / 100 MHz
- LVTTL Interface
- Burst read/write operation and burst read/ single write operation capability
- Programmable burst length ;
  1, 2, 4, 8, Full page
- Programmable burst sequence
  Sequential / Interleave
- Full Page burst length capability
  Sequential burst
  Burst stop capability
- Programmable $\overline{CAS}$ Latency ; 1, 2, 3
- CKE power down mode
- Input / Output data masking
- 4096 Refresh Cycles / 64ms
- Auto refresh / Self refresh Capability
- Serial Presence Detect with EEPROM

- **GMM2642227DNTG** (Both Side)



Pin Name

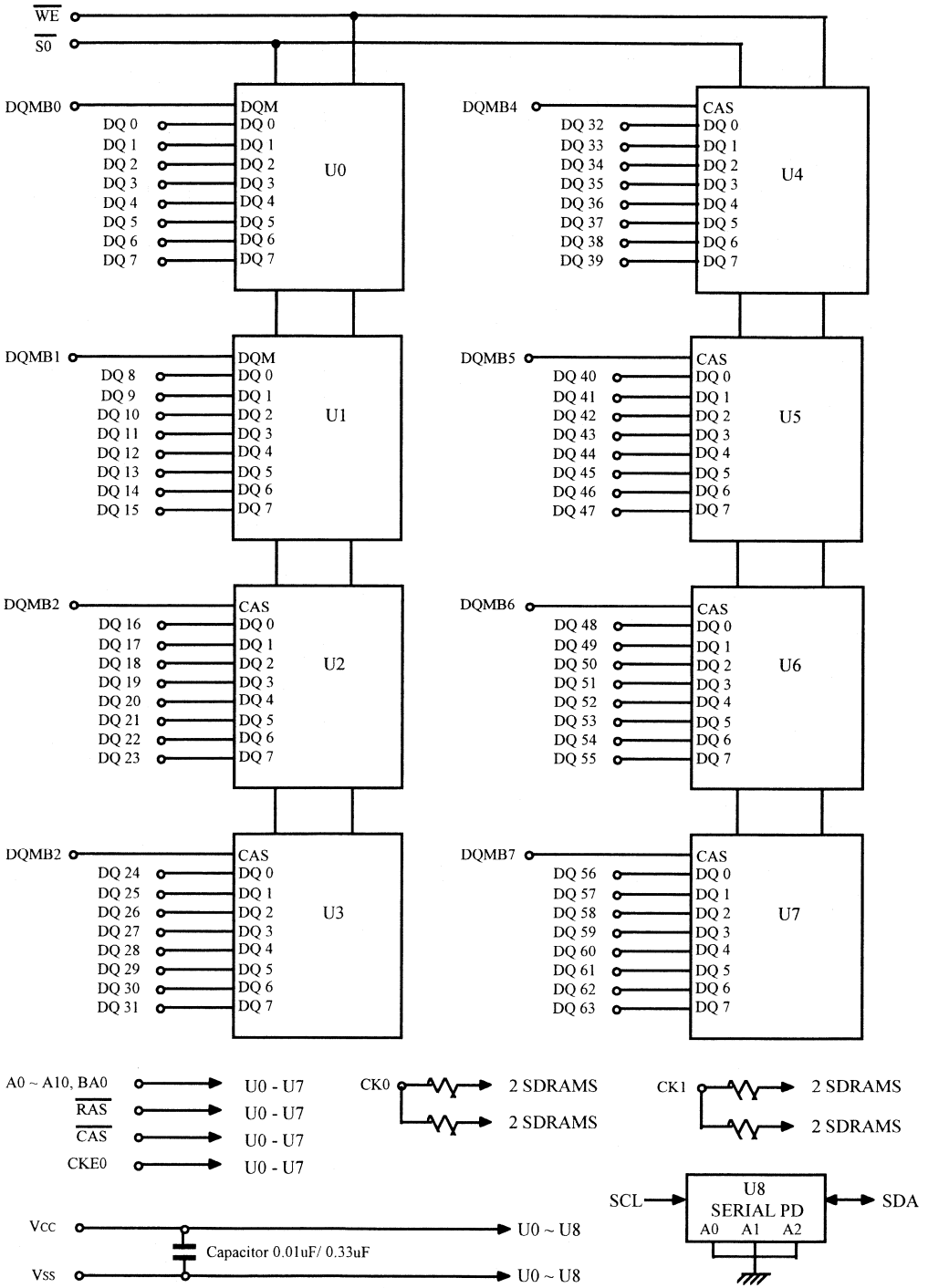
CK0,1	Clock inputs
$\overline{CKE0}$	Clock Enable
$\overline{S0}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0~A10	Address input
BA0	Bank Address input
DQ0~63	Data input / output
DQMB0~7	Data input / output Mask
V_{CC}	Power for internal circuit
V_{SS}	Ground for internal circuit
NC	No Connect
V_{REF}	Power Supply for Reference
SDA	Serial Data input / output
SCL	Serial Clock
DU	Don't Use

Pin Configuration

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	25	DQMB1	49	DQ13	73	NU	97	DQ22	121	DQ24
2	Vss	26	DQMB5	50	DQ45	74	CK1	98	DQ54	122	DQ56
3	DQ0	27	Vcc	51	DQ14	75	Vss	99	DQ23	123	DQ25
4	DQ32	28	Vcc	52	DQ46	76	Vss	100	DQ55	124	DQ57
5	DQ1	29	A0	53	DQ15	77	NC	101	Vcc	125	DQ26
6	DQ33	30	A3	54	DQ47	78	NC	102	Vcc	126	DQ58
7	DQ2	31	A1	55	Vss	79	NC	103	A6	127	DQ27
8	DQ34	32	A4	56	Vss	80	NC	104	A7	128	DQ59
9	DQ3	33	A2	57	NC	81	Vcc	105	A8	129	Vcc
10	DQ35	34	A5	58	NC	82	Vcc	106	BA0	130	Vcc
11	VDD	35	Vss	59	NC	83	DQ16	107	Vss	131	DQ28
12	VDD	36	Vss	60	NC	84	DQ48	108	Vss	132	DQ60
13	DQ4	37	DQ8	61	CK0	85	DQ17	109	A9	133	DQ29
14	DQ36	38	DQ40	62	CKE0	86	DQ49	110	BA1*	134	DQ61
15	DQ5	39	DQ9	63	Vcc	87	DQ18	111	A10/AP	135	DQ30
16	DQ37	40	DQ41	64	Vcc	88	DQ50	112	A11*	136	DQ62
17	DQ5	41	DQ10	65	$\overline{RAS}$	89	DQ19	113	Vcc	137	DQ31
18	DQ38	42	DQ42	66	CAS	90	DQ51	114	Vcc	138	DQ63
19	DQ7	43	DQ11	67	$\overline{WE}$	91	Vss	115	DQMB2	139	Vss
20	DQ39	44	DQ43	68	CKE1*	92	Vss	116	DQMB6	140	Vss
21	Vss	45	Vcc	69	$\overline{S0}$	93	DQ20	117	DQMB3	141	SDA
22	Vss	46	Vcc	70	A12	94	DQ52	118	DQMB7	142	SCL
23	DQMB0	47	DQ12	71	S1	95	DQ21	119	Vss	143	Vcc
24	DQMB4	48	DQ44	72	A13	96	DQ53	120	Vss	144	Vcc

* These pins are not used in this module

Block Diagram



Pin Description

Pin Name	DESCRIPTION
CK0,1 (input pins)	CK is the master clock input to this pin. The other input signals are referred at CK rising edge.
CKE0 (input pins)	This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.
$\overline{S0}$ (input pins)	When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (input pins)	Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.
A0 ~ A10 (input pins)	Row address (AX0 to AX10) is determined by A0 to A10 level at the bank active command cycle CK rising edge. Column address is determined by A0 to A8 level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, both banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by BA0 is precharged.
BA0 (input pin)	BA0 is a bank select signal. If BA0 is Low, bank 0 is selected, and if BA0 is High , bank 1 is selected.
DQ0 ~ DQ63 (I/O pins)	Data is input and output from these pins. These pins are the same as those of a conventional DRAMs.
DQMB0 ~ DQMB7 (input pins)	DQMB controls input/output buffers. • Read operation: If DQMB is High, The output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z. • Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.
V_{CC} (power supply pins)	3.3 V is applied. (V_{CC} is for the internal circuit)
V_{SS} (power supply pins)	Ground is connected. (V_{SS} is for the internal circuit)
NC	No Connection pins.

SERIAL PRESENCE DETECT INFORMATION

- Serial PD Interface Protocol : I^2C
- Current sink capability of SDA driver $\leq$ 3mA
- Maximum clock frequency : 100KHz

Byte No.	Function description	Function support	Hex Value	Note
0	# of bytes written into serial memory at module manufacturer	128 bytes	80h	
1	Total # of bytes of SPD memory device	256 bytes(2K-bit)	08h	
2	Fundamental memory type	SDRAM	04h	
3	# of row addresses on this assembly	11	0Bh	1
4	# of column addresses on this assembly	9	09h	2
5	# of module banks on this assembly	1 banks	01h	
6	Data width of this assembly	64 bits	40h	
7	.....Data width of this assembly(Continued)	N/A	00h	
8	Voltage interface standard of this assembly	LVTTL	01h	
9	SDRAM cycle time	10ns	A0h	3, 8
		12ns	C0h	3, 8
10	SDRAM access time from clock	7.5ns	75h	4, 8
		9ns	90h	4, 8
11	DIMM configuration type	Non-parity	00h	
12	Refresh rate/type	4096/64ms : Normal	00h	
13	DRAM/SDRAM width, Primary DRAM	x8	08h	
14	Error checking DRAM data width	none	00h	
15	Minimum clock delay, Back to Back Random Column Address	t_{CCD} = 1CLK	01h	
16	Burst lengths supported	1, 2, 4, 8 & full page	8Fh	6
17	# of banks on each SDRAM device	2 banks	02h	
18	$\overline{CAS}$ Latency	$\overline{CAS}$ Latency = 1, 2 & 3	07h	7
19	$\overline{CS}$ Latency	$\overline{CS}$ latency = 0	01h	
20	Write Latency	Write latency = 0	01h	
21	SDRAM Module Attributes	Unbuffer	00h	

Byte No.	Function description	Function support	Hex Value	Note
22	SDRAM device attributes : General		0Fh	5
23	Minimum Clock Cycle Time at CL X-1	t_{CK2}=15ns	F0h	
24	Maximum Data Access Time from Clock @CL X-1	t_{AC2}=9.5ns	95h	
		t_{AC2}=9ns	90h	
25	Minimum Clock Cycle Time at CL X-2	t_{CK1}=30ns	78h	
26	Maximum Data Access Time from Clock @CL X-2	t_{AC1}=27ns	6Ch	
27	Minimum Row Precharge Time	t_{RP}=30ns	1Eh	
28	Minimum Row Active to Row Active Delay	t_{RRD}=20ns	14h	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay	t_{RCD}=30ns	1Eh	
30	Minimum $\overline{RAS}$ Pulse Width	t_{RAS}=60ns	3Ch	
31	Module Bank Density	16MBytes	04h	
32~61	Superset Information(may be used in future)		00h	
62	SPD Revision	Rev.1	01h	
63	Checksum for bytes 0 ~ 62		A3h	
64	Manufacturer JEDEC ID code per JEP-106E	Continuation Code	7Fh	
65		LGS	E0h	
66~71			00h	
72	Manufacturer location	Korea	52h	
73	Manufacturer 's part number	G(GMM2642227DNTG-10K/J)	47h	
74	Allowed characters 0-9, a-z and space	M	4Dh	
75		M	4Dh	
76		2	32h	
77		6	36h	
78		4	34h	
79		2	32h	
80		2	32h	
81		2	32h	
82		7	37h	

Byte No.	Function description	Function support	Hex Value	Note
83		B	42h	
84		N	4Eh	
85		T	54h	
86		G	47h	
87		-	2Dh	
88		1	31h	
89		0	30h	
90		K	4Bh	
91~92	Revision Code	Initial release (Rev.0)	00h	
93	Date Code	WW	00h	
94		YY	00h	
95~98	Assembly Serial Number	Binary incremental	00h	
99~125	Manufacturer Specific Data	N/A	00h	
126	Intel specfication CAS# Latency Support	66MHz	66h	
127	Manufacturing Date		06h	
128~255	Reserved		00h	

- Above data are based on the SPD specification of JEDEC standard and can be changed.

- Note : 1. If the bank select address of RA11 is excluded, this byte must be programmed by 0Bh.
  2. If the bank select address of CA11 is excluded, this byte must be programmed by 0Ah
  3. In case of - 10 part, the minimum cycle time is 10ns, 15ns and 30ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
     So, the value of A0h is based on the minimum cycle time @ $\overline{CAS}$ latency = 3.
     In case of - 12 part, the minimum cycle time is 12ns, 18ns and 36ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
     So, the value of C0h is based on the minimum cycle time @ $\overline{CAS}$ latency = 3.

4. In case of - 10 part, the access time is 7.5ns, 9.5ns and 27ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 75h is based on the access time @ $\overline{CAS}$ latency = 3.
   In case of - 12 part, the access time is 9ns, 12ns and 32ns @ $\overline{CAS}$ latency = 3, 2 and 1 respectively.
   So, the value of 90h is based on the access time @ $\overline{CAS}$ latency = 3.
5. LGS' SDRAM supports Burst Read Single-bit Write, Precharge all and Auto precharge functions.
   If Burst Read Single-bit Write function is not supports, this byte must be programmed by 06h.
6. LGS' SDRAM supports burst lengths of 1, 2, 4, 8 and full page. If burst lengths of 1 and 4 are only supports, this byte must be programmed by 05h.
7. LGS' SDRAM supports $\overline{CAS}$ latency of 1, 2 and 3. If $\overline{CAS}$ latency of 2 and 3 are only supported, this byte must be programmed by 06h.
8. This value is based on the component specification.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	-0.5 to +4.6	V	1
Supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V	1
Short circuit output current	I_{OUT}	50	mA	
Power dissipation	P_D	8	W	
Operating temperature	Topr	0 to +65	℃	
Storage temperature	Tstg	-55 to +125	℃	

Notes : 1. Respect to V_{SS}

Recommended DC Operating Conditions (Ta = 0 to + 65℃)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.6	V	1
	V_{SS}, V_{SSQ}	0	0	V	
Input high voltage	V_{IH}	2.0	4.6	V	1, 2
Input low voltage	V_{IL}	-0.3	0.8	V	1, 3

Notes : 1. All voltage referred to V_{SS}.

2. V_{IH} (max) = 5.5V for pulse width $\leq$ 5ns

3. V_{IL} (min) = -1.0V for pulse width $\leq$ 5ns

DC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ±0.3V, V_{SS}, V_{SSQ}= 0V)

Parameter	Symbol	- 10		- 12		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	-	800	-	680	mA	Burst length=1 t_{RC}=min	1, 2, 4
Standby current (Bank Disable)	I_{CC2}	-	24	-	24	mA	CKE=V_{IL}, t_{CK}=min	5
		-	16	-	16	mA	CKE=V_{IL} CLK=V_{IL} or V_{IH} Fixed	6
		-	240	-	200	mA	CKE=V_{IH}, NOP command t_{CK}=15ns	3
Active standby current (Bank Active)	I_{CC3}	-	56	-	56	mA	CKE=V_{IL}, t_{CK}=min I/O = High-Z	1, 2
		-	280	-	240	mA	CKE=V_{IH} NOP command t_{CK}=min I/O = High-Z	1, 2, 3
Burst operating current (CL=2)	I_{CC4}	-	800	-	680	mA	t_{CK}=min BL = 4	1, 2, 4
Burst operating current (CL=3)	I_{CC4}	-	1200	-	1000	mA		
Auto Refresh current	I_{CC5}	-	680	-	560	mA	t_{RC}=min	
Self refresh current	I_{CC6}	-	16	-	16	mA	$V_{IH} \geq V_{CC}$ - 0.2 0V ≤ V_{IL} ≤0.2V	7
Input leakage current	I_{LI}	-10	10	-10	10	μA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	-10	10	-10	10	μA	$0 \leq Vout \leq V_{CC}$ I/O = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH}=-2mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	I_{OL}=2mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signal transition is once per two CLK cycles.
4. Input signal transition is once per two CLK cycle.
5. After power down mode, CLK operating current.
6. After power down mode, no CLK operating current.
7. After self refresh mode set, self refresh current.

Capacitance (Ta = 25℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V)

Symbol	Parameter	Min	Max	Unit	Notes
C_{I1}	Input capacitance (A0 ~ A10, BA0)	-	50	pF	1, 3
C_{I2}	Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE)	-	45	pF	1, 3
C_{I3}	Input capacitance (CK0 ~ CK1)	-	45	pF	1, 3
C_{I4}	Input capacitance ($\overline{S0}$)	-	45	pF	1, 3
C_{I5}	Input capacitance (DQMB0 ~ DQMB7)	-	15	pF	1, 3
$C_{I/O}$	Input / output capacitance (DQ0 ~ DQ63)	-	15	pF	1, 2, 3

Note : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. DQMB = V_{IH} to disable Dout.
3. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

Parameter		Symbol	-10		-12		Unit	Notes
			Min	Max	Min	Max		
System clock cycle time	(CL=1)	t_{CK}	30	-	36	-	ns	1
	(CL=2)	t_{CK}	15	-	18	-		
	(CL=3)	t_{CK}	10	-	12	-		
CLK high pulse width		t_{CKH}	3	-	4	-	ns	1
CLK low pulse width		t_{CKL}	3	-	4	-	ns	1
Access time from CLK	(CL=1)	t_{AC}	-	27	-	32	ns	1, 2, 6
	(CL=2)	t_{AC}	-	9.5	-	12		
	(CL=3)	t_{AC}	-	8	-	9.5		
Data-out hold time		t_{OH}	3	-	3	-	ns	1,2
CLK to Data-out low impedance		t_{LZ}	0	-	0	-	ns	1,2,3
CLK to Data-out high impedance	(CL=1)	t_{HZ}	-	13	-	15	ns	1, 4
	(CL=2, 3)	t_{HZ}	-	7	-	9		
Data-in setup time		t_{DS}	2	-	3	-	ns	1
Data-in hold time		t_{DH}	1	-	1	-	ns	1
Address setup time		t_{AS}	2	-	3	-	ns	1
Address hold time		t_{AH}	1	-	1	-	ns	1

AC Characteristics (Ta = 0 to 65℃, V_{CC}, V_{CCQ} = 3.3V ± 0.3V, V_{SS}, V_{SSQ} = 0V)

(Continued)

Parameter	Symbol	- 10		- 12		Unit	Notes
		Min	Max	Min	Max		
CKE setup time	t_{CES}	2	-	3	-	ns	1, 5
CKE setup time for power down exit	t_{CESP}	2	-	3	-	ns	1
CKE hold time	t_{CEH}	1	-	1	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) setup time	t_{CS}	2	-	3	-	ns	1
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM) hold time	t_{CH}	1	-	1	-	ns	1
Ref/Active to Ref/Active command period	t_{RC}	90	-	108	-	ns	1
Active to Precharge command period	t_{RAS}	60	120000	72	120000	ns	1
Active to Precharge on full page mode	t_{RASC}	-	120000	-	120000	ns	1
Active command to column command (same bank)	t_{RCD}	30	-	36	-	ns	1
Precharge to active command period	t_{RP}	30	-	36	-	ns	1
The last data-in to Precharge lead time	t_{RWL}	15	-	18	-	ns	1
Active (a) to Active (b) command period	t_{RRD}	20	-	24	-	ns	1
Transition time (rise to fall)	t_T	1	5	1	5	ns	
Refresh period	t_{REF}	-	64	-	64	ms	

Notes : 1. AC measurement assumes t_T = 1ns. Reference level for timing of input signals is 1.40V.

2. Access time is measured at 1.40V. Load condition is C_L = 50pF with current source.

3. t_{LZ} (max)defines the time at which the outputs achieves the low impedance state.

4. t_{HZ} (max)defines the time at which the outputs achieves the high impedance state.

5. t_{CES} define CKE setup time to CKE rising edge except power down exit command.

6. -10 grade products are classified as follows.

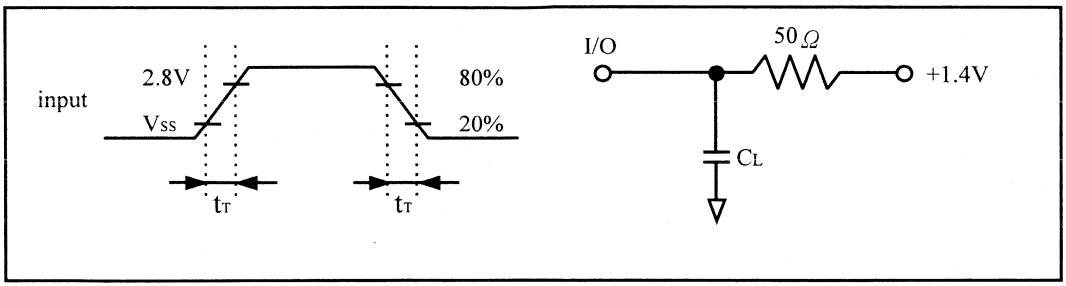
① 10K is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9ns.

② 10J is the product that meets t_{CK}=15ns, C.L=2, t_{AC}=9.5ns.

③ 10 is the product that meets the LGS SDRAM spec.

Test Condition

- Input and output-timing reference levels: 1.4V
- Input waveform and output load: See following figures



Relationship Between Frequency and Minimum Latency.

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
Active command to column command (same bank)		t_{RCD}	3	2	1	3	2	1	
Active command to active command period (same bank)		t_{RC}	9	6	3	9	6	3	= [t_{RAS}+t_{RP}]
Active command to precharge command (same bank)		t_{RAS}	6	4	2	6	4	2	
Precharge command to active command (same bank)		t_{RP}	3	2	1	3	2	1	
Last data input to precharge command (same bank)		t_{RWL}	2	1	1	2	1	1	
Active command to active command (different bank)		t_{RRD}	2	2	1	2	2	1	
Self refresh exit time		I_{SREX}	2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)		I_{APW}	5	3	2	5	3	2	= [t_{RWL}+t_{RP}]
Self refresh exit to command input		I_{SEC}	9	6	3	9	6	3	= [t_{RC}]
Precharge command to high impedance	(CL=3)	I_{HZP}	3	3	3	3	3	3	
	(CL=2)	I_{HZP}	-	2	2	-	2	2	
	(CL=1)	I_{HZP}	-	-	1	-	-	1	
Last data out to active command (auto precharge) (same bank)		I_{APR}	1	1	1	1	1	1	
Last data out to precharge (early precharge)	(CL=3)	I_{EP}	-2	-2	-2	-2	-2	-2	
	(CL=2)	I_{EP}	-	-1	-1	-	-1	-1	
	(CL=1)	I_{EP}	-	-	0	-	-	0	
Column command to column command		I_{CCD}	1	1	1	1	1	1	
Write command to data in latency		I_{WCD}	0	0	0	0	0	0	
DQM to data in		I_{DID}	0	0	0	0	0	0	
DQM to data out		I_{DOD}	2	2	2	2	2	2	

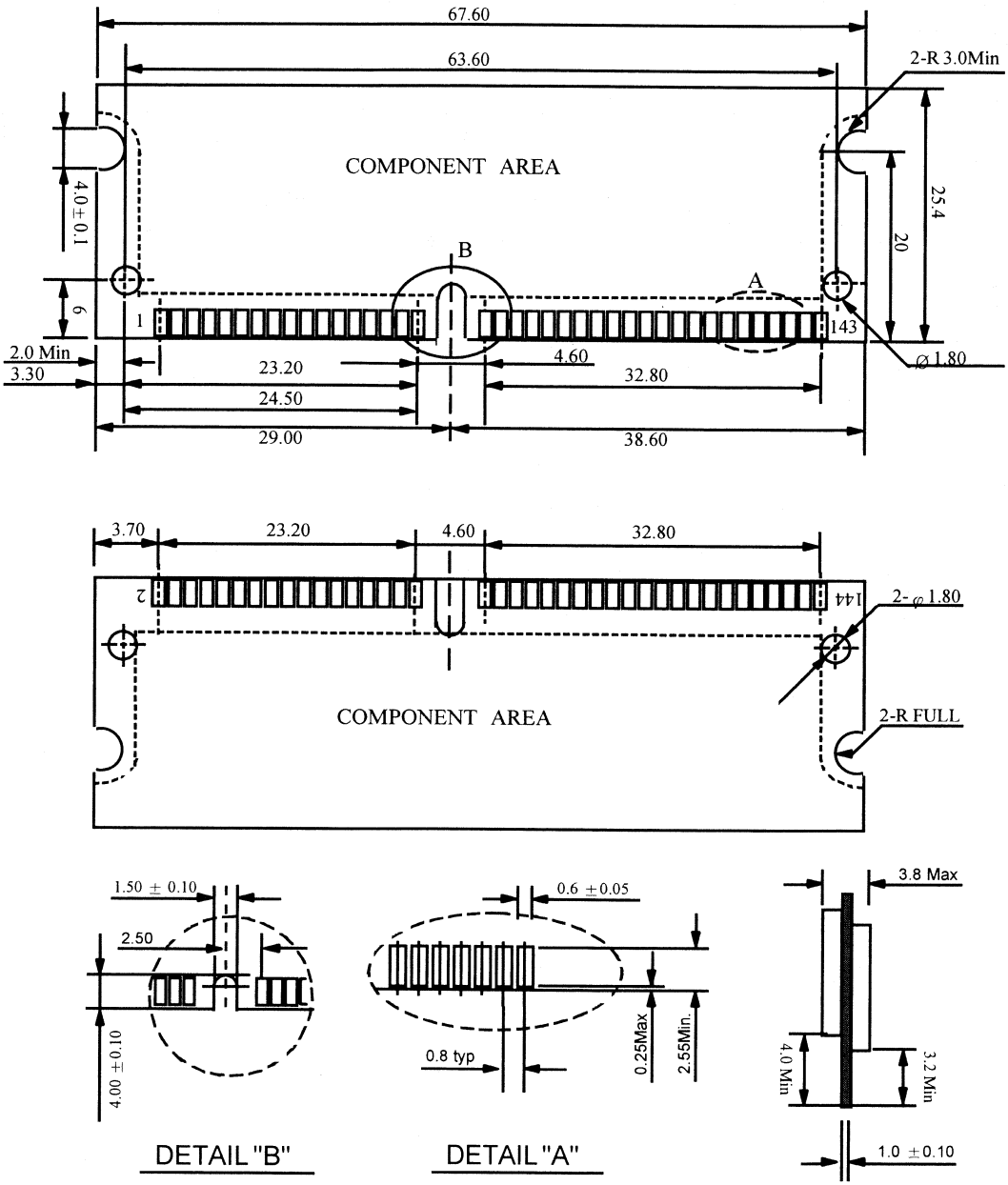
Relationship Between Frequency and Minimum Latency. (Continued)

Parameter		Symbol	- 10			- 12			Notes
Frequency (MHz)			100	66	33	83	55	28	
t_{CK} (ns)			10	15	30	12	18	36	
CKE to CLK disable		I_{CLE}	1	1	1	1	1	1	
Register set to active command		t_{RSA}	1	1	1	1	1	1	
CS to command disable		I_{CDD}	0	0	0	0	0	0	
Power down exit to command input		I_{PEC}	1	1	1	1	1	1	
Burst stop to output valid data hold	(CL=3)	I_{BSR}	2	2	2	2	2	2	
	(CL=2)	I_{BSR}	-	1	1	-	1	1	
	(CL=1)	I_{BSR}	-	-	0	-	-	0	
Burst stop to output high impedance	(CL=3)	I_{BSH}	3	3	3	3	3	3	
	(CL=2)	I_{BSH}	-	2	2	-	2	2	
	(CL=1)	I_{BSH}	-	-	1	-	-	1	
Burst stop to write data ignore		I_{BSW}	0	0	0	0	0	0	

Notes : 1. t_{RCD} to t_{RRD} are recommended value.
2. CL = $\overline{CAS}$ Latency
3. 2clock is required between self refresh exit time and next refresh or active command.

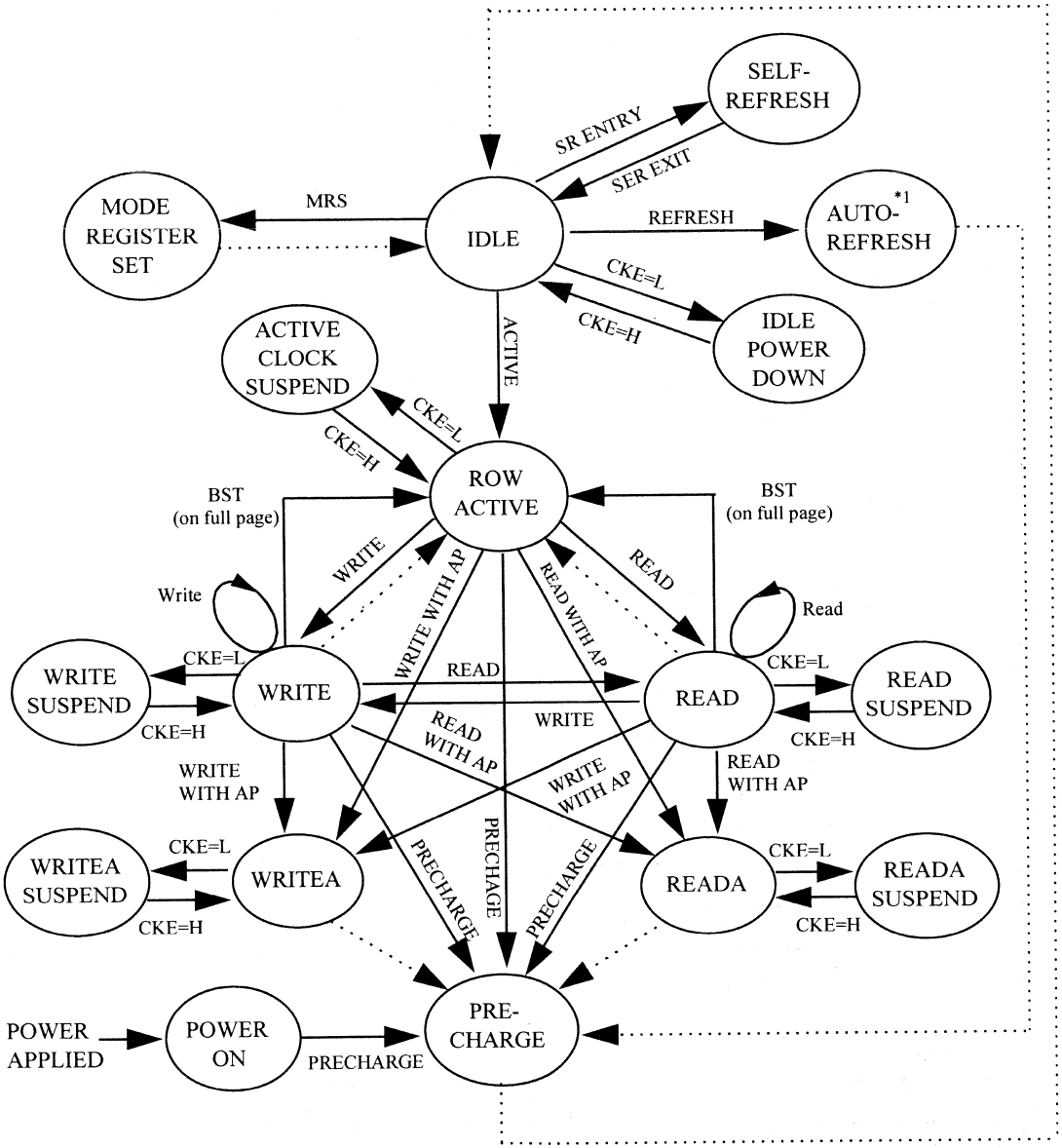
Package Dimension

Unit: mm



NOTE : 1. Tolerances on all dimensions ±0.15 unless otherwise specified.
2. Thickness(* Mark) includes Plating and / or Metallization.

16M SDRAM Function State Diagram



Note: 1. After the auto-refresh operation, precharge is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A11) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

• A11, A10, A9, A8: (OPCODE):

The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

• Burst read and BURST WRITE:

Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

• Burst read and SINGLE WRITE:

Data is only written to the column address specified during the write cycle, regardless of the burst length.

• A7:

Keep this bit Low at the mode register set cycle.

• A6, A5, A4: (LMODE):

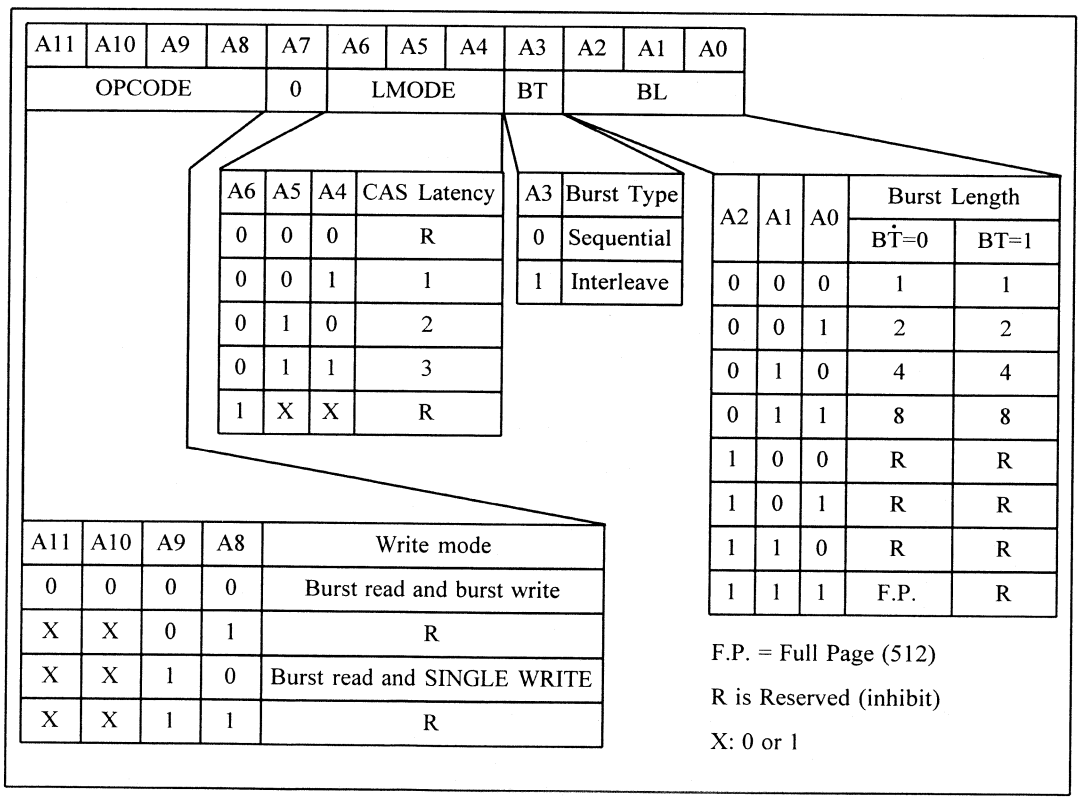
These pins specify the $\overline{CAS}$ latency.

• A3: (BT):

A burst type is specified . When full-page burst is performed, only "sequential" can be selected.

• A2, A1, A0: (BL):

These pins specify the burst length.



A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE				0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	1
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A11	A10	A9	A8	Write mode
0	0	0	0	Burst read and burst write
X	X	0	1	R
X	X	1	0	Burst read and SINGLE WRITE
X	X	1	1	R

F.P. = Full Page (512)

R is Reserved (inhibit)

X: 0 or 1

Burst Sequence

Burst Length	Starting Column Address A2 A1 A0	Sequential	Interleave
2	X X 0	0 - 1	0 - 1
	X X 1	1 - 0	1 - 0
4	X 0 0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
	X 0 1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
	X 1 0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
	X 1 1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8	0 0 0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	0 0 1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
	0 1 0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
	0 1 1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
	1 0 0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	1 0 1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
	1 1 0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
	1 1 1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0

Operation of 16M SDRAM Series

Read / Write Operation

• **Bank active:** Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Either bank 0 or bank 1 is activated according to the status of the A11 pin, and the row address (AX0 to AX10) is activated by the A0 to A10 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

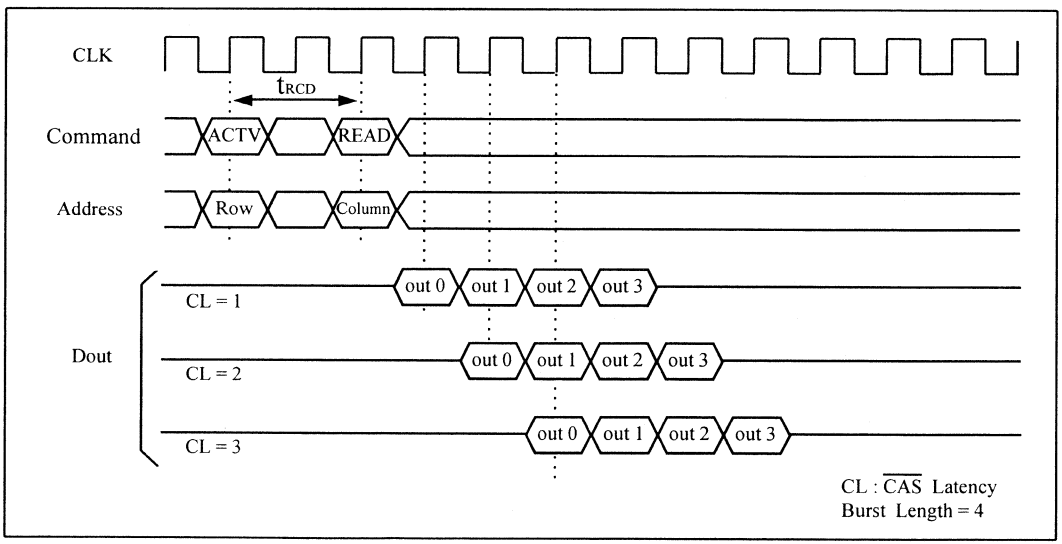
• **Read operation:** A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set.

GM72V16821DT series can perform a burst read operation. The burst length can be set to 1, 2, 4, 8 or full page(512). The start address for a burst read is specified by the column address (AY0 to AY8) and the bank select address (A11) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 1, 2, 3.
When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

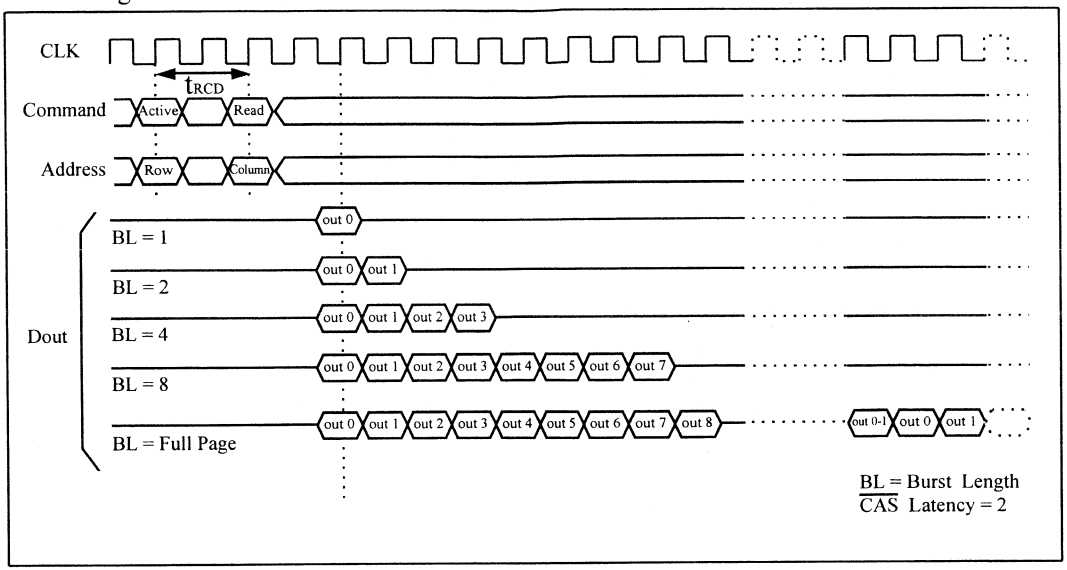
When the burst length is full-page (512), data is repeatedly output until the burst stop command is input.

The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



Burst Length



• Write Operation

Burst write or single write mode is selected by the OPCODE(A11, A10, A9, A8) of the mode register.

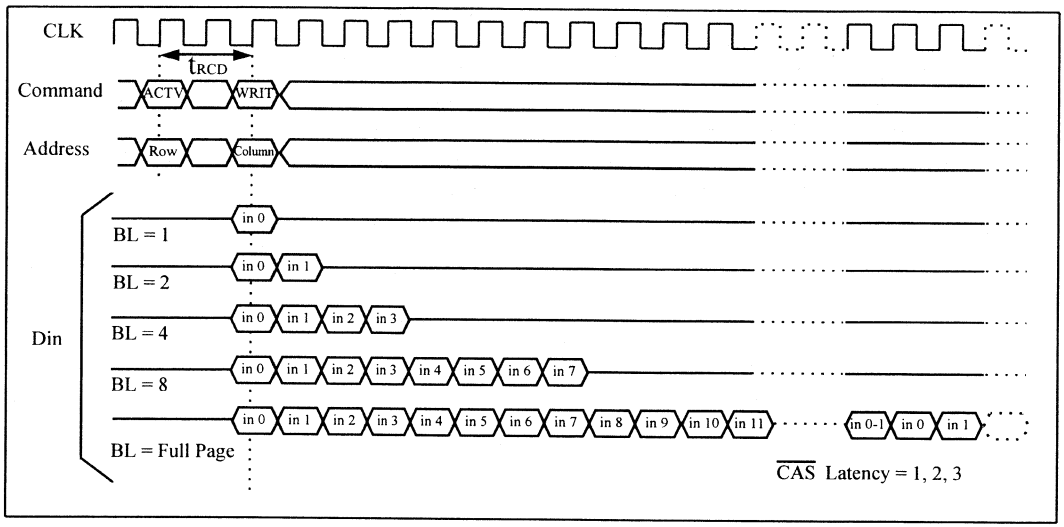
1. Burst write:

A burst write operation is enabled by setting OPCODE(A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8 and full page, like burst read operations. The write start address is specified by the column address (AY0 TO AY8) and the bank select address (A11) at the write command set cycle.

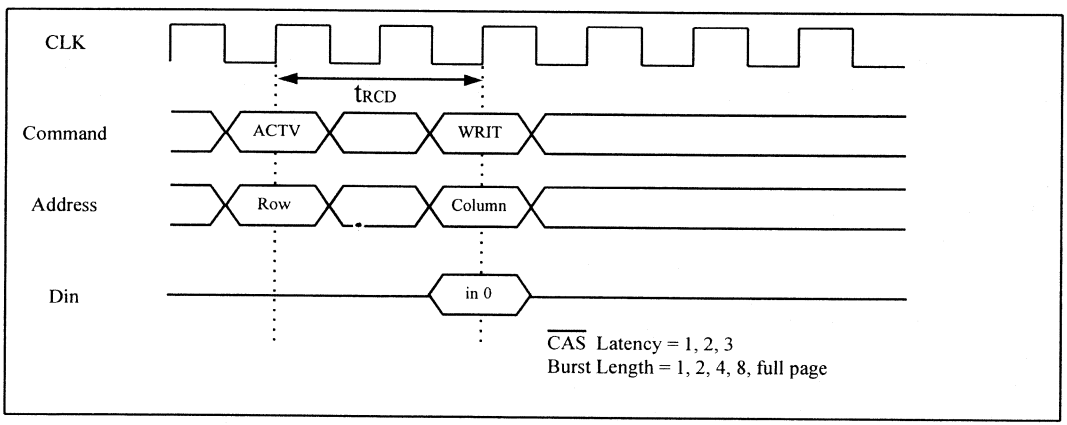
2. Single write:

A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY8) and the bank select address (A11) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0.)

Burst Write



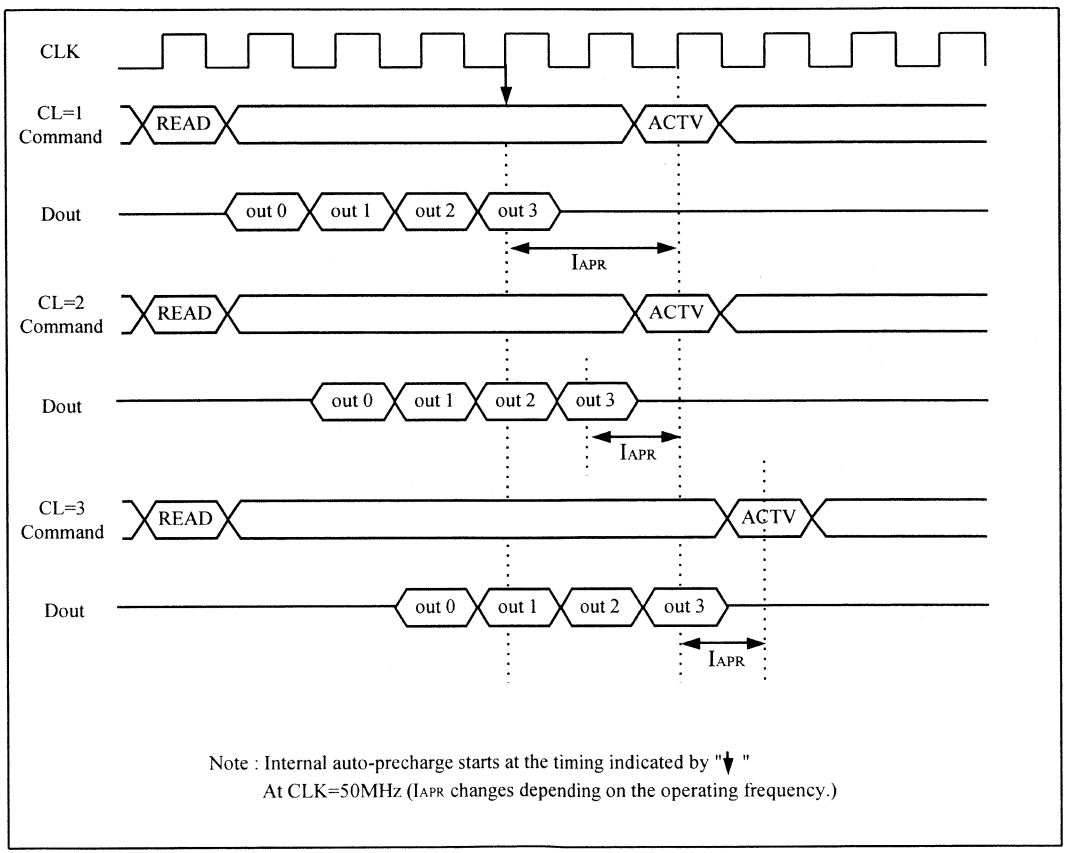
Single Write



• **Read with auto-precharge:** In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by I_{APR} is required before execution of the next command.

$\overline{CAS}$ Latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output
1	same cycle as the final data is output

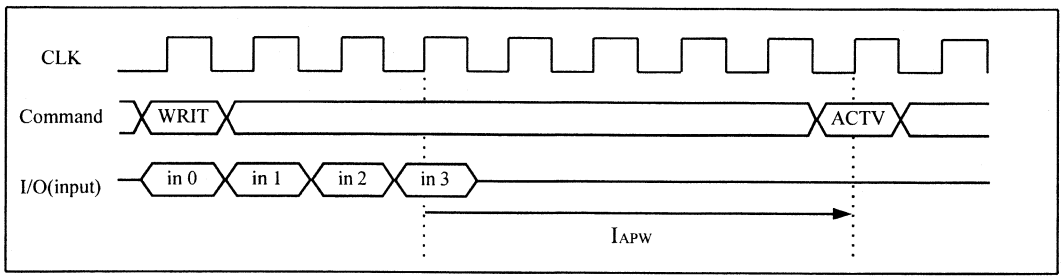
Burst Read with Auto-precharge



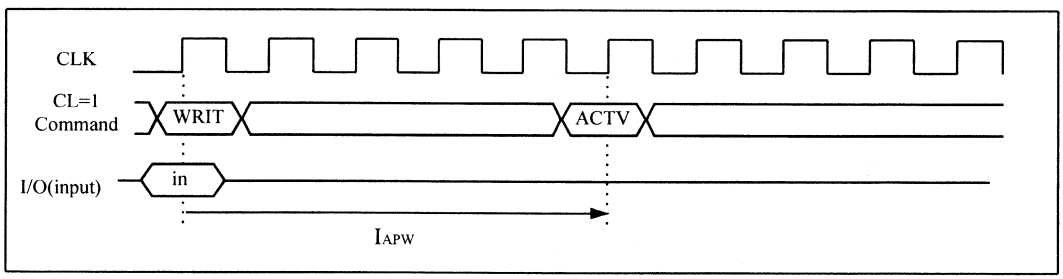
Note : Internal auto-precharge starts at the timing indicated by "▼"
At CLK=50MHz (I_{APR} changes depending on the operating frequency.)

• **Write with auto-precharge:** In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of I_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write



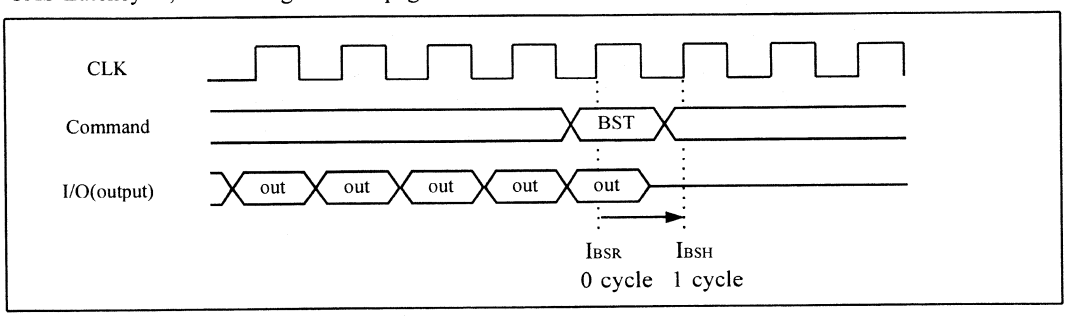
Full-page Burst Stop

• **Burst stop command during burst read:** The burst stop (BST) commnad is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read.

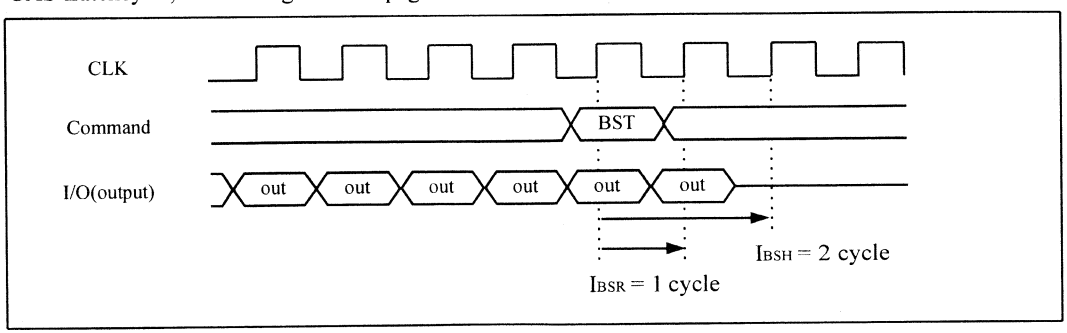
The timing from command input to the last data changes depending on the $\overline{CAS}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4, and 8.

$\overline{CAS}$ Latency	BST to valid data	BST to high impedance
1	0	1
2	1	2
3	2	3

$\overline{CAS}$ Latency=1, Burst Length = full page

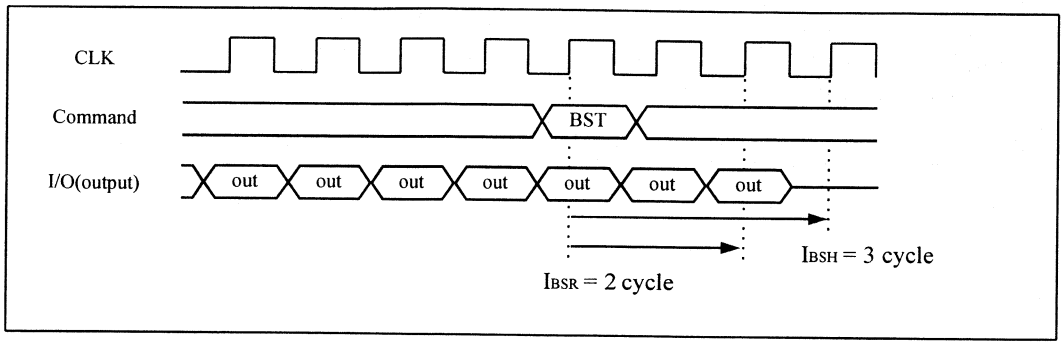


$\overline{CAS}$ Latency=2, Burst Length = full page



Full-page Burst Stop

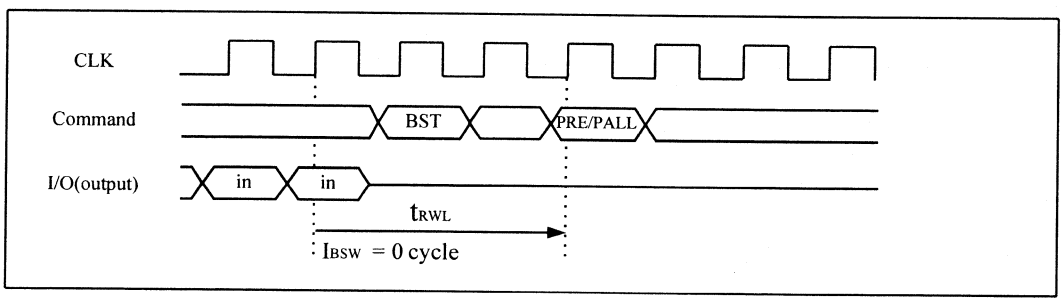
$\overline{CAS}$ Latency = 3, Burst Length = full page



• **Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command, and in subsequent cycles.

In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8. And an interval of t_{RWL} is required between the BST command and the next precharge command.

Burst Length = full page



Command Intervals

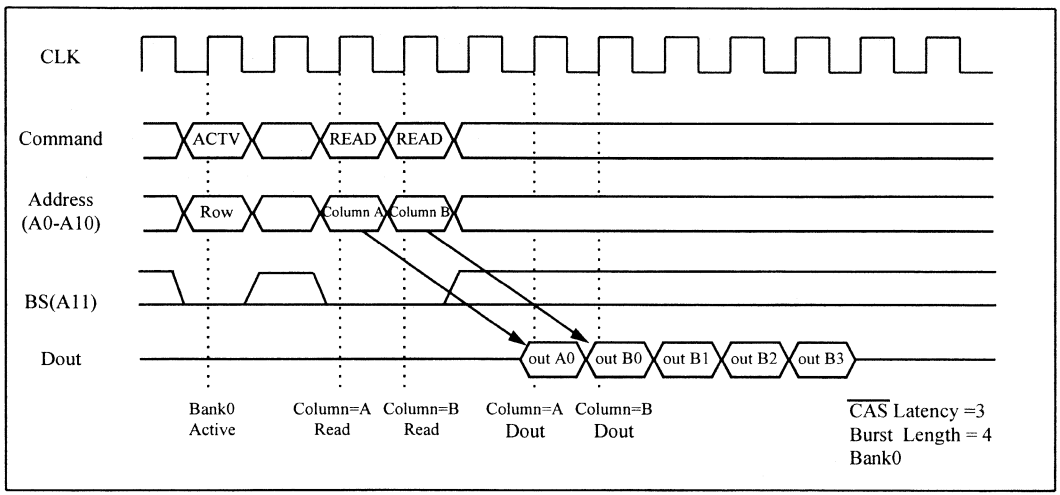
• Read command to Read command interval:

1. Same bank, same ROW address:

When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle.

Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (same Row address in same bank)



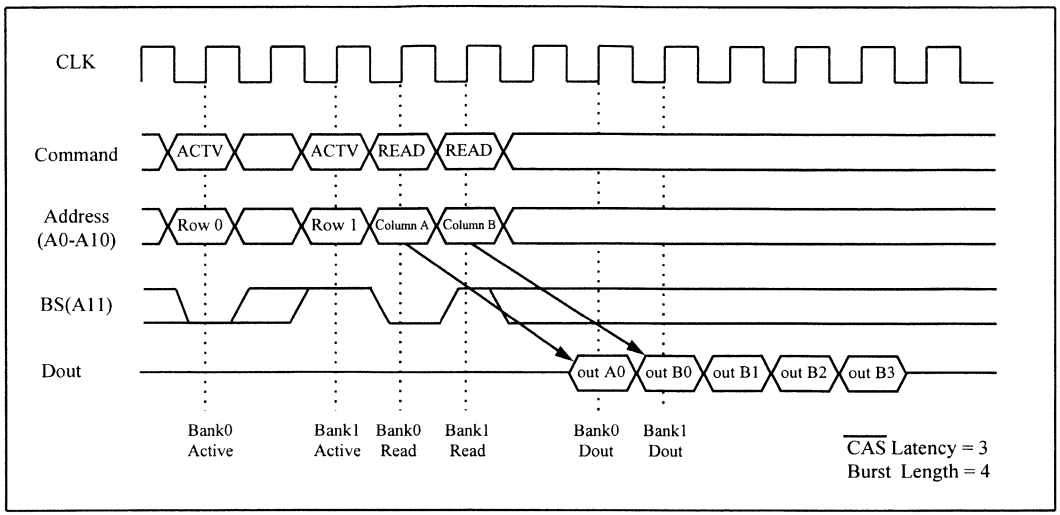
2. Same bank, different ROW address:

When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to seperate the two read commands with a precharge command and a bank-active command.

3. Different bank:

When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (different bank)



Command Intervals

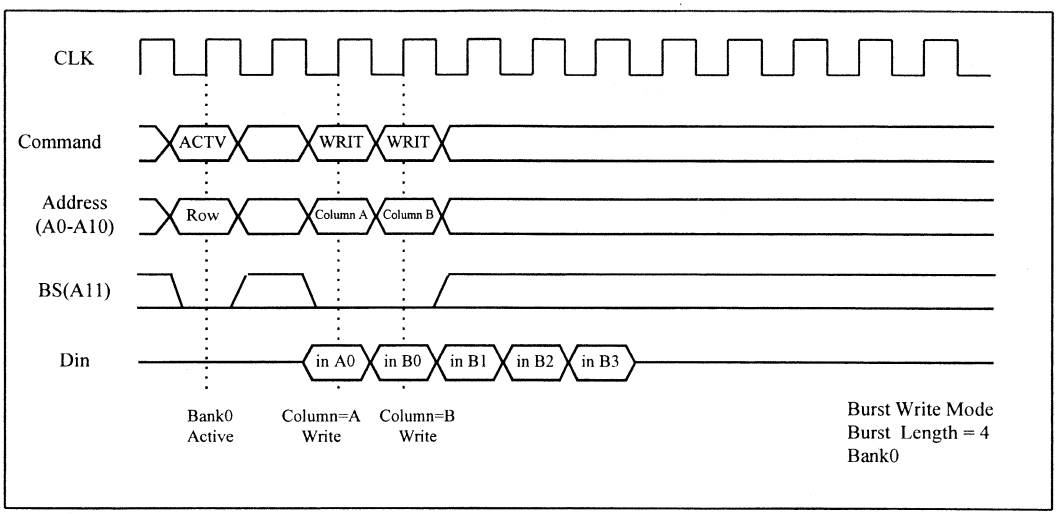
• Write command to Write command interval:

1. Same bank, same ROW address:

When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle.

In the case of burst writes, the second write command has priority.

WRITE to WRITE Command Interval (same ROW address in same bank)



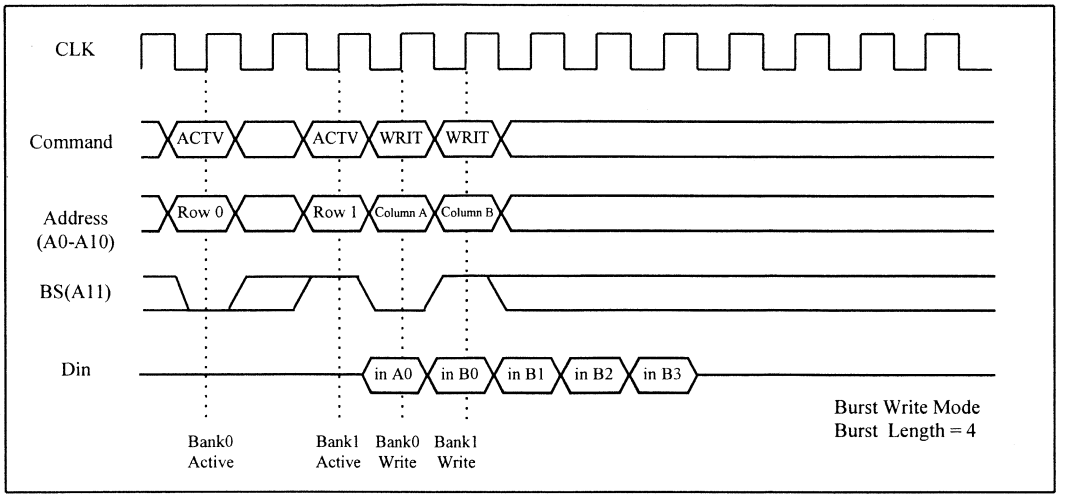
2. Same bank, different ROW address:

When the ROW address changes, consecutive read commands cannot be executed; it is necessary to seperate the two write commands with a precharge command and a bank-active command.

3. Different bank:

When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE command interval (different bank)

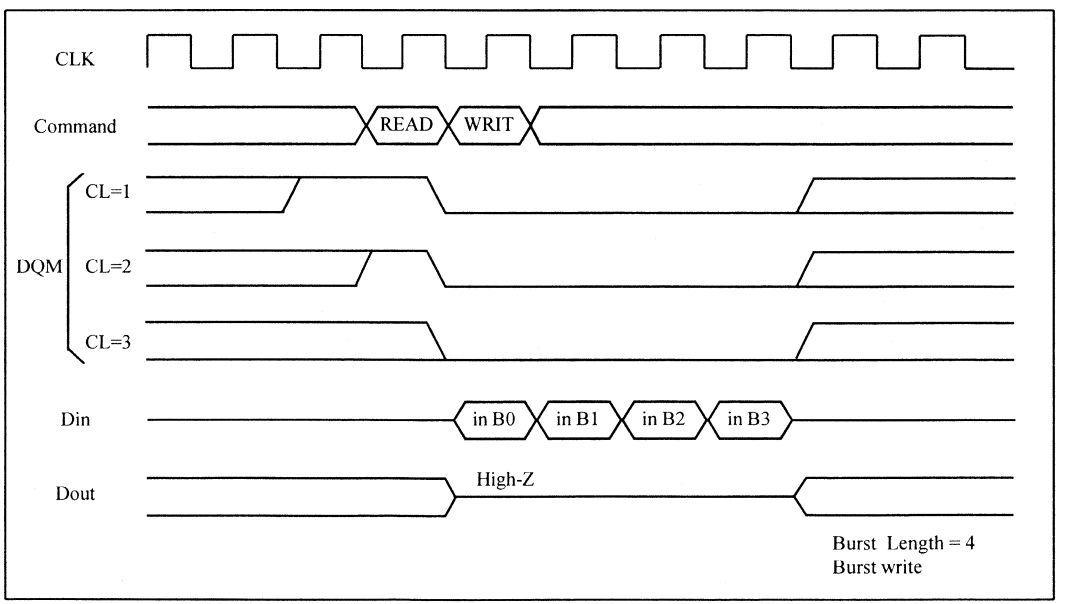


• **Read command to Write command interval:**

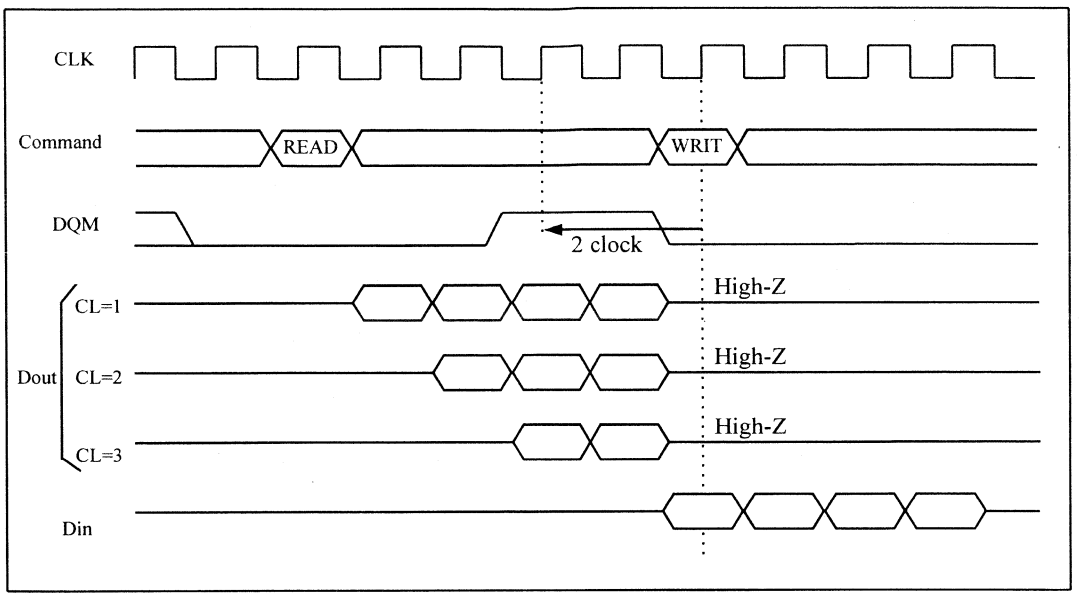
1. **Same bank, same Row address:**

When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM must be set High-Z so that the ouput buffer becomes High-Z before data input.

READ to WRITE command interval (1)



READ to WRITE command interval (2)



2. Same bank, different ROW address:

When the ROW address changes, consecutive write commands cannot be executed; it is necessary to seperate the two write commands with a precharge command or a bank-active command.

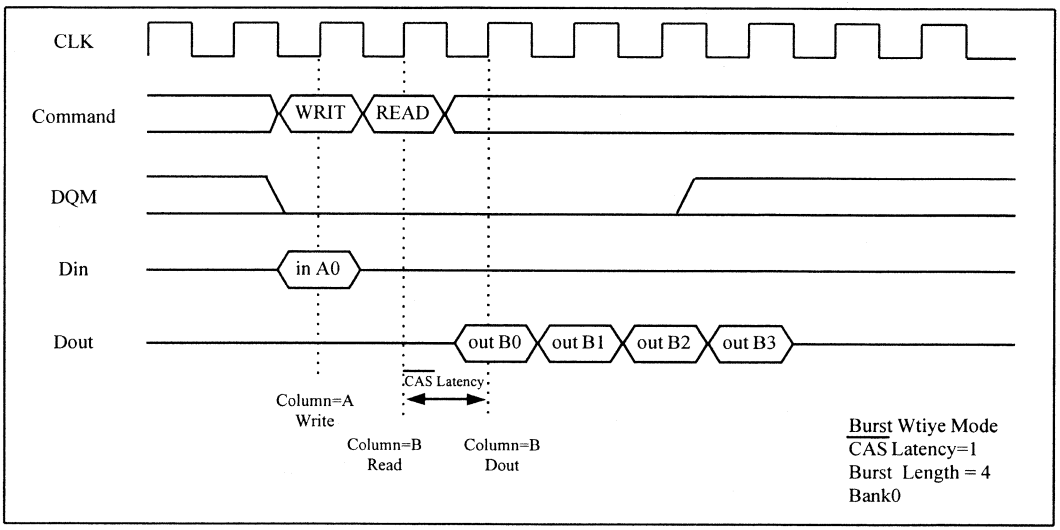
3. Different bank:

When the bank changes, the write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM must be set High so that the output buffer becomes High-Z before data input.

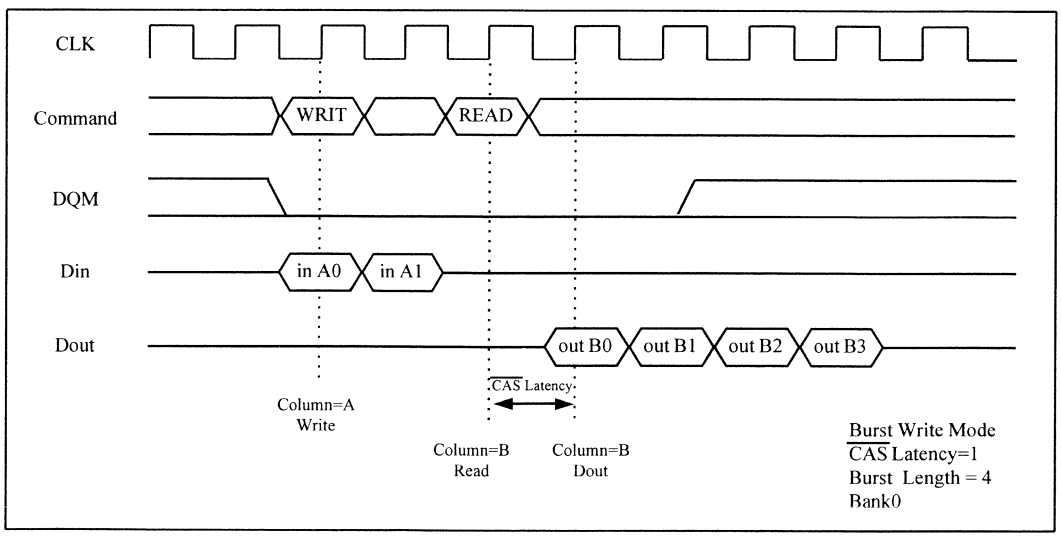
• **Write command to Read command interval:**

1. **Same bank, same Row address:** When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



2. **Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

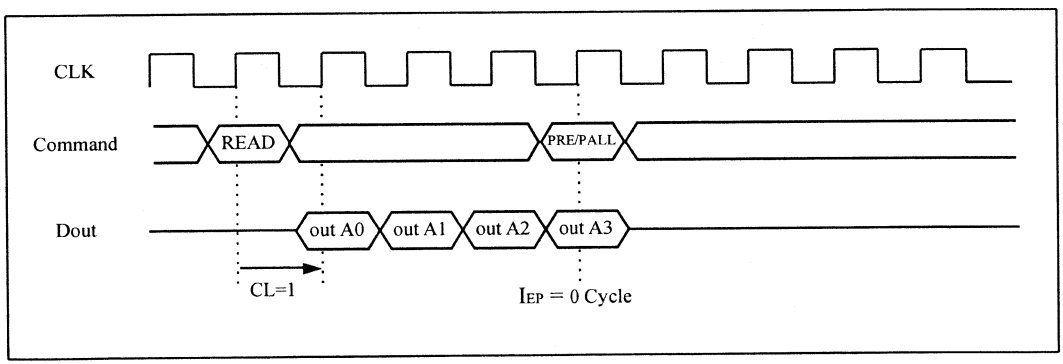
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed(as in the case of the same bank and the same address).

• **Read command to Precharge interval (same bank):** When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by I_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read.

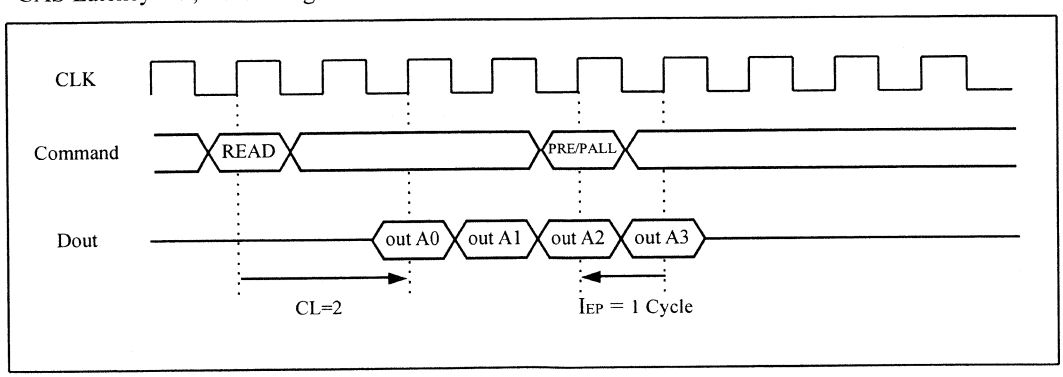
To read all data by burst read, the cycles defined by I_{EP} must be assured as an interval from the final data output to precharge command execution.

• **READ to PRECHARGE Command Interval (same bank) : To output all data**

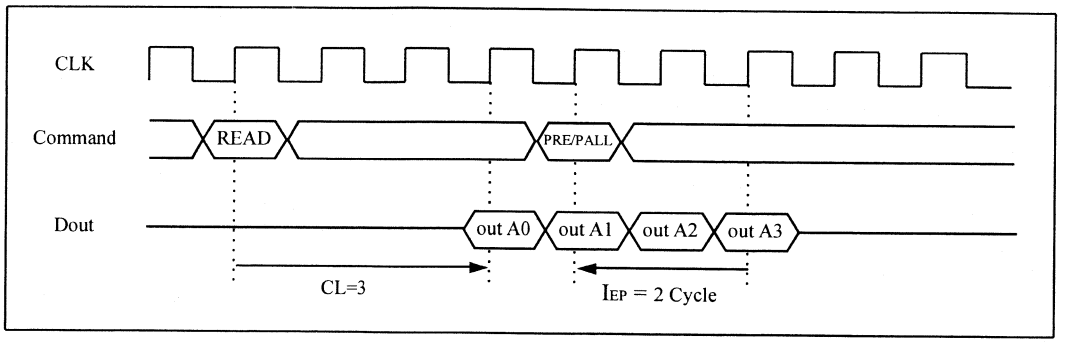
$\overline{CAS}$ Latency = 1, Burst Length = 4



$\overline{CAS}$ Latency = 2, Burst Length = 4

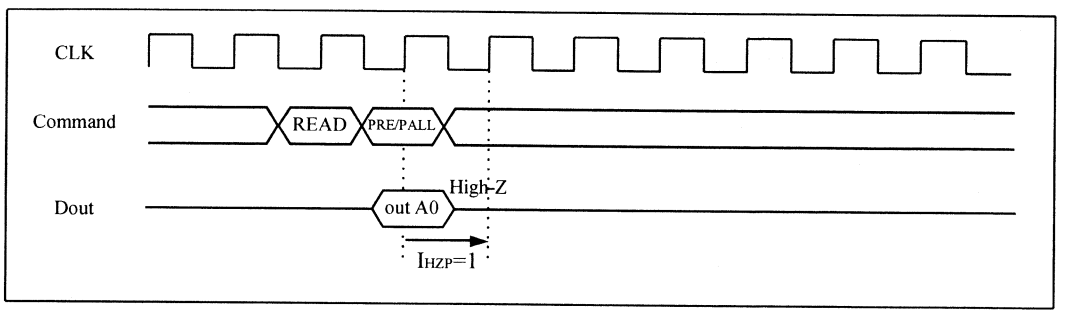


$\overline{CAS}$ Latency = 3, Burst Length = 4

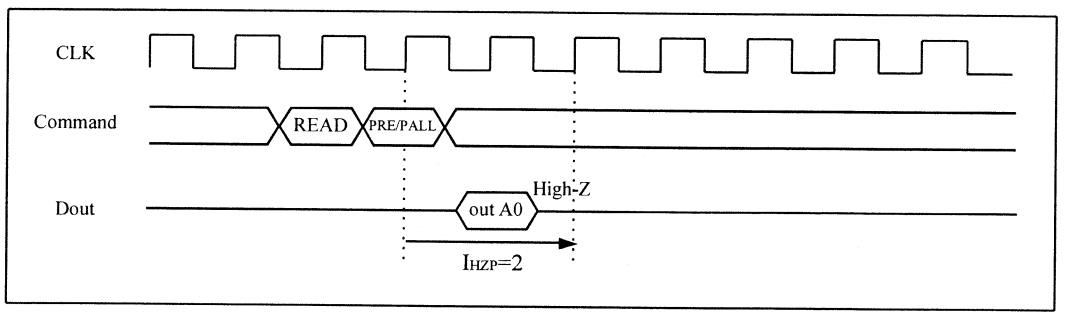


• **READ to PRECHARGE Command interval (same bank) : To stop output data**

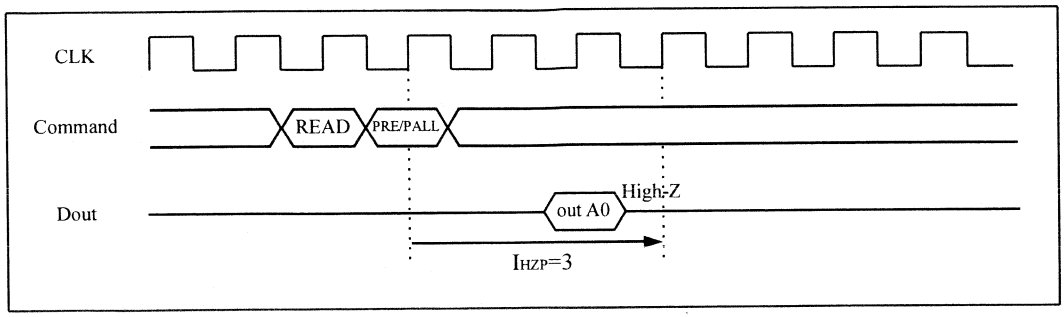
$\overline{CAS}$ Latency = 1, Burst length = 1, 2, 4, 8



$\overline{CAS}$ Latency = 2, Burst length = 1, 2, 4, 8



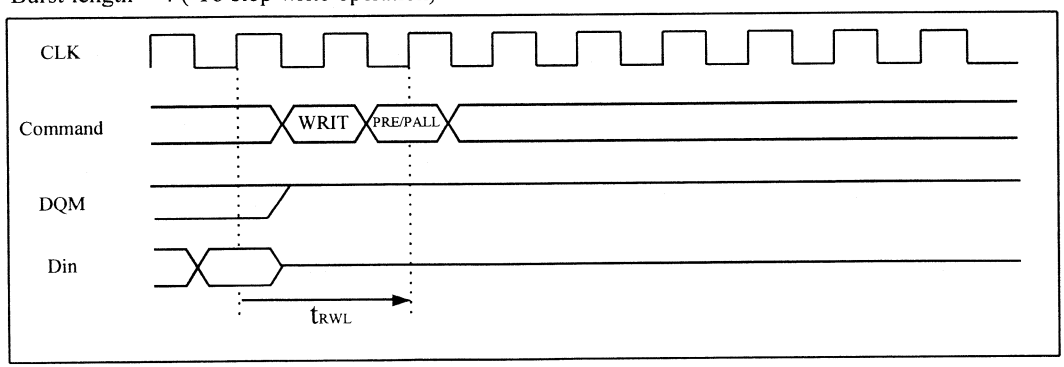
$\overline{\text{CAS}}$ Latency = 3, Burst Length = 1, 2, 4, 8

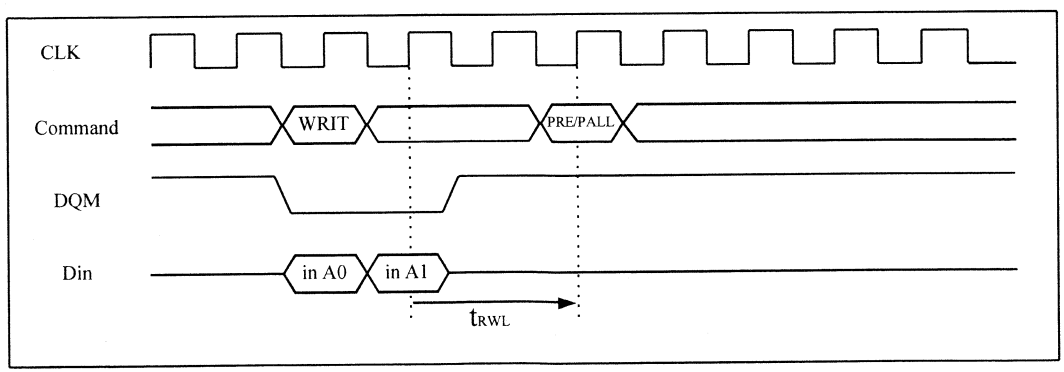


• **Write command to Precharge command interval (same bank):** When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQM for assurance of the cycle defined by t_{RWL}.

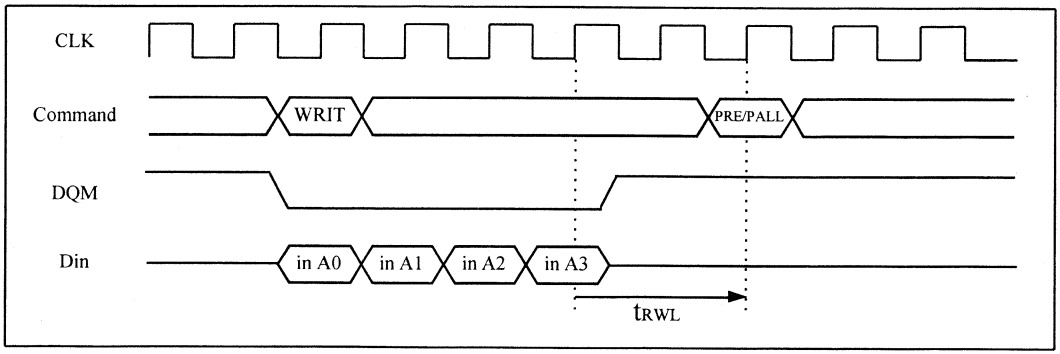
• **WRITE to PRECHARGE Command Interval (same bank)**

Burst length = 4 (To stop write operation)





Burst Length = 4 (To write all data)

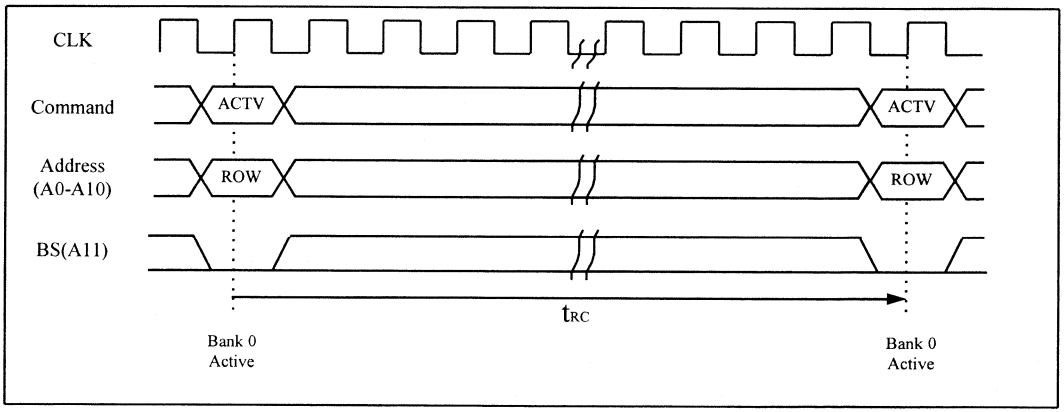


• **Bank Active command interval**

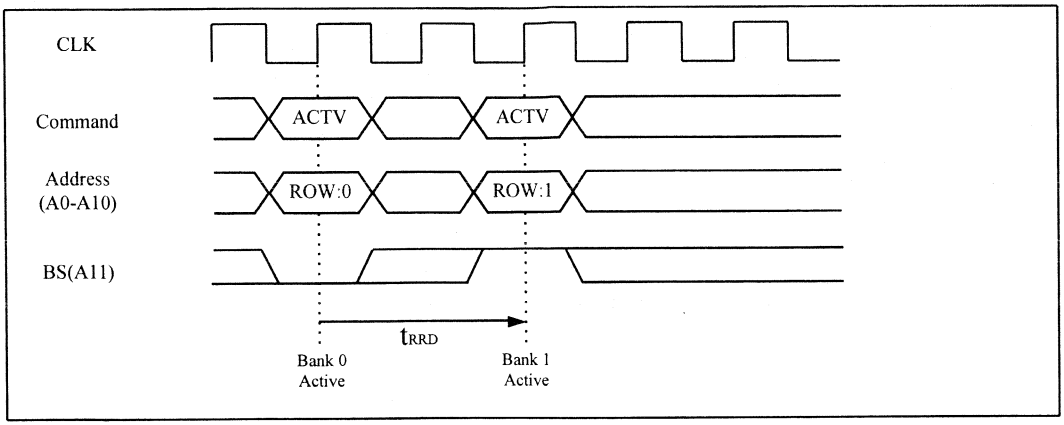
1. **Same bank:** The interval between the two bank-active commands must be no less than t_{RC}.

2. **In the case of different bank-active commands:** The interval between the bank-active commands must be no less than t_{RRD}.

Bank Active to Bank Active command interval for same bank

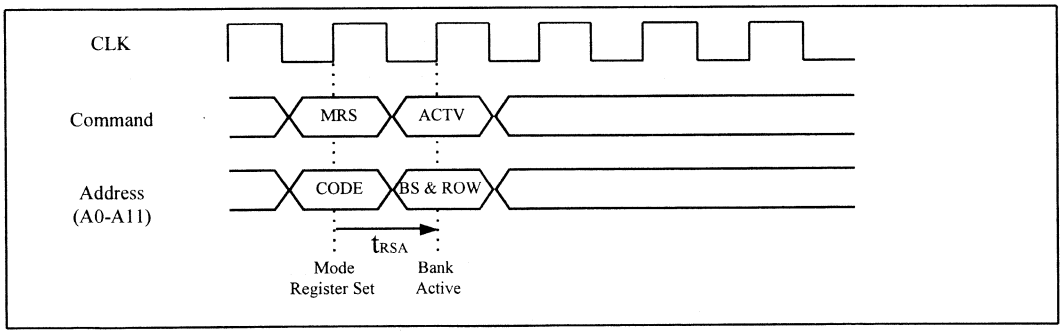


Bank active to bank active for different bank



- **Mode Register Set to Bank -active command interval**

The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



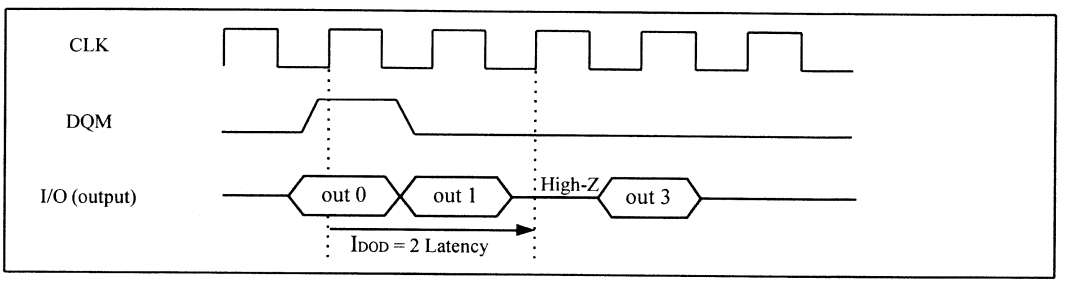
DQM Control

The DQM mask the lower and upper bytes of I/O data, respectively. The timing of DQM is different during reading and writing.

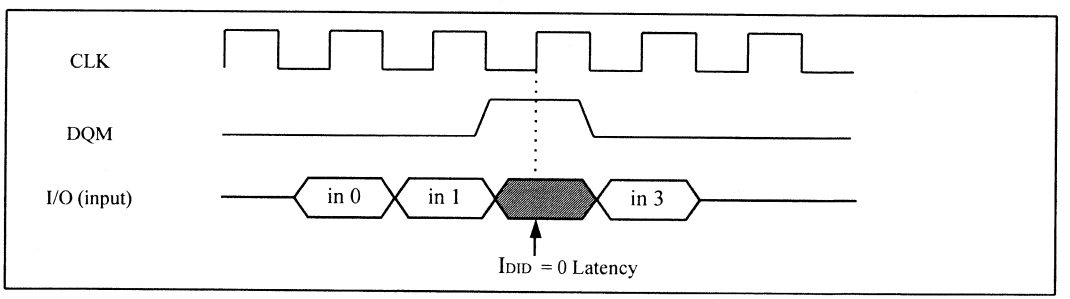
• **Reading:** When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is **2**.

• **Writing:** Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is **0**.

Reading



Writing



Refresh

• Auto refresh:

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4,096 cycles/64ms. (4,096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

• Self refresh:

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. After the self-refresh, since it is impossible to determine the address of the last ROW to be refreshed, an auto-refresh should immediately be performed for all addresses (4,096 cycles).

Others

• Power down mode:

The synchronous DRAM enters power down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

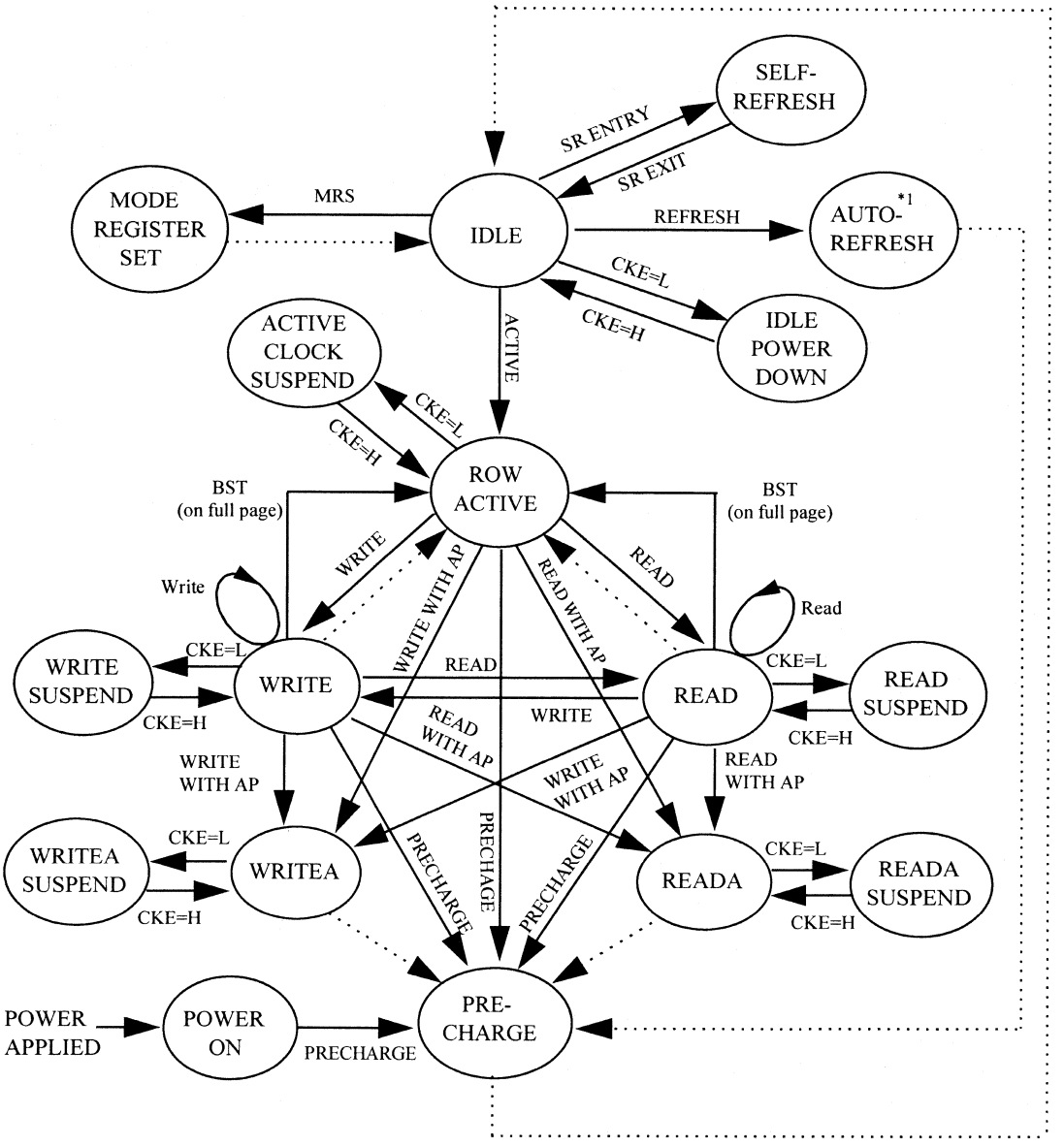
• Clock suspend (Active power down) mode:

By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained (bank-active or read/write operation is suspended). When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

• Power-up sequence:

During power-up sequence, the DQM and the CKE must be set to High. When $200\mu s$ has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

64M SDRAM Function State Diagram



Note: 1. After the auto-refresh operation, precharge is performed automatically and enter the IDLE state.

Mode Register Configuration

The mode register is set by the inpit to the address pins (A0 to A13) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

• **A13, A12, A11, A10, A9, A8: (OPCODE):**

The synchronous DRAM has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

• **Burst read and BURST WRITE:**

Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

• **Burst read and SINGLE WRITE:**

Data is only written to the column address specified during the write cycle, regardless of the burst length.

• **A7:**

Keep this bit Low at the mode register set cycle.

• **A6, A5, A4: (LMODE):**

These pins specify the $\overline{\text{CAS}}$ latency.

• **A3: (BT):**

A burst type is specified . When full-page burst is performed, only "sequential" can be selected.

• **A2, A1, A0: (BL):**

These pins specify the burst length.

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE						0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	R
0	1	0	2
0	1	1	3
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A13	A12	A11	A10	A9	A8	Write mode
0	0	0	0	0	0	Burst read and BURST WRITE
X	X	X	X	0	1	R
X	X	X	X	1	0	Burst read and SINGLE WRITE
X	X	X	X	1	1	R

F.P. = Full Page (256:GM72V661641CT)
(512:GM72V66841CT)
(1024:GM72V66441CT)
R is Reserved (inhibit)
X: 0 or 1

Burst Sequence

Burst Length	Starting Column Address	Addressing(decimal)	
	A2 A1 A0	Sequential	Interleave
2	V V 0	0 - 1	0 - 1
	V V 1	1 - 0	1 - 0
4	V 0 0	0 - 1 - 2 - 3	0 - 1 - 2 - 3
	V 0 1	1 - 2 - 3 - 0	1 - 0 - 3 - 2
	V 1 0	2 - 3 - 0 - 1	2 - 3 - 0 - 1
	V 1 1	3 - 0 - 1 - 2	3 - 2 - 1 - 0
8	0 0 0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7
	0 0 1	1 - 2 - 3 - 4 - 5 - 6 - 7 - 0	1 - 0 - 3 - 2 - 5 - 4 - 7 - 6
	0 1 0	2 - 3 - 4 - 5 - 6 - 7 - 0 - 1	2 - 3 - 0 - 1 - 6 - 7 - 4 - 5
	0 1 1	3 - 4 - 5 - 6 - 7 - 0 - 1 - 2	3 - 2 - 1 - 0 - 7 - 6 - 5 - 4
	1 0 0	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3	4 - 5 - 6 - 7 - 0 - 1 - 2 - 3
	1 0 1	5 - 6 - 7 - 0 - 1 - 2 - 3 - 4	5 - 4 - 7 - 6 - 1 - 0 - 3 - 2
	1 1 0	6 - 7 - 0 - 1 - 2 - 3 - 4 - 5	6 - 7 - 4 - 5 - 2 - 3 - 0 - 1
	1 1 1	7 - 0 - 1 - 2 - 3 - 4 - 5 - 6	7 - 6 - 5 - 4 - 3 - 2 - 1 - 0

* Notes : V : Valid Address

Operation of 64M SDRAM Series

Read / Write Operation

• **Bank active:** Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Bank 0, bank 1, bank 2 or bank 3 is activated according to the status of the A12/A13 pin, and the row address (AX0 to AX11) is activated by the A0 to A11 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

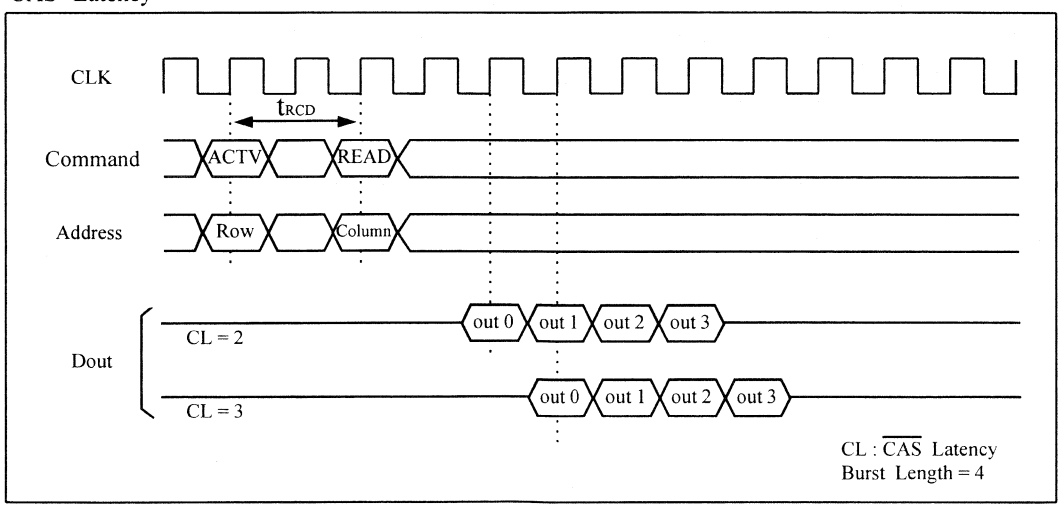
• **Read operation:** A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CAS}$ Latency - 1) cycle after read command set. GM72V661641CT, GM72V66841CT, GM72V66441CT can perform a burst read operation.

The burst length can be set to 1, 2, 4, 8 or full page(256;GM72V661641CT, 512;GM72V66841CT, 1024;M72V66441CT). The start address for a burst read is specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) at the read command set cycle. In a read operation, data output starts after the number of cycles specified by the $\overline{CAS}$ Latency. The $\overline{CAS}$ Latency can be set to 2 or 3.
When the burst length is 1, 2, 4, or 8, the Dout buffer automatically becomes High-Z at the next cycle after the successive burst-length data has been output.

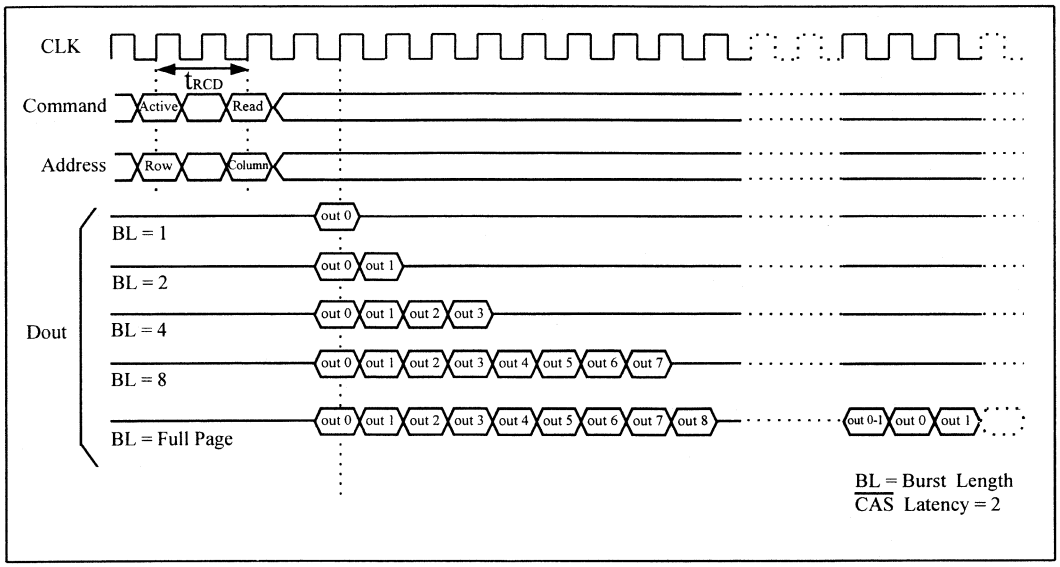
When the burst length is full-page (256;GM72V661641CT, 512;GM72V66841CT, 1024;M72V66441CT), data is repeatedly output until the burst stop command is input.

The $\overline{CAS}$ latency and burst length must be specified at the mode register.

$\overline{CAS}$ Latency



Burst Length



• Write Operation

Burst write or single write mode is selected by the OPCODE(A13, A12,A11, A10, A9, A8) of the mode register.

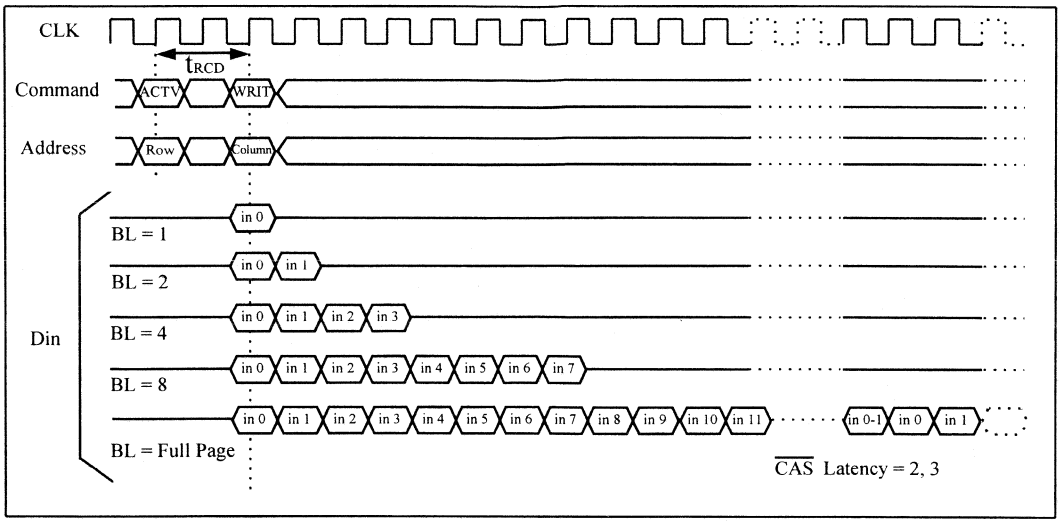
1. Burst write:

A burst write operation is enabled by setting OPCODE(A9, A8) to (0, 0). A burst write starts in the same cycle as a write command set. (The latency of data input is 0.) The burst length can be set to 1, 2, 4, 8 and full page, like burst read operations. The write start address is specified by the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) at the write command set cycle.

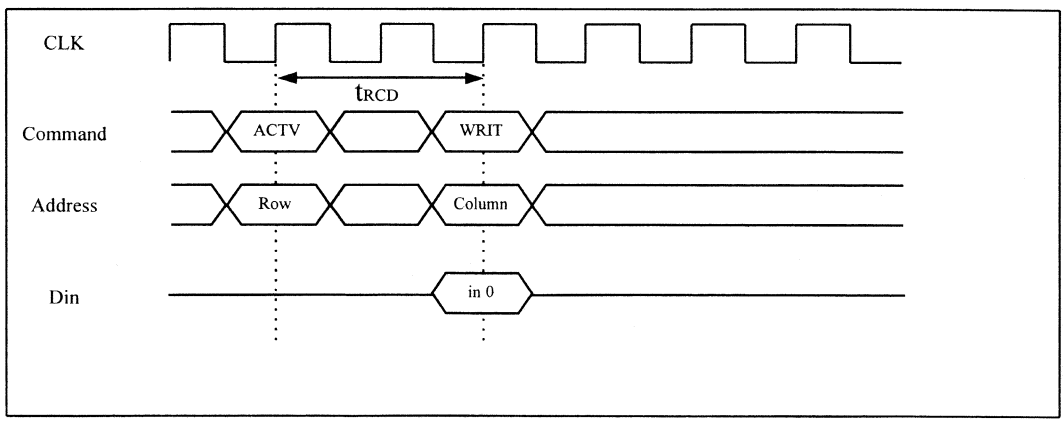
2. Single write:

A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address (AY0 to AY7; GM72V661641CT, AY0 to AY8; GM72V66841CT, AY0 to AY9; GM72V66441CT) and the bank select address (A12/A13) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0.)

Burst Write



Single Write

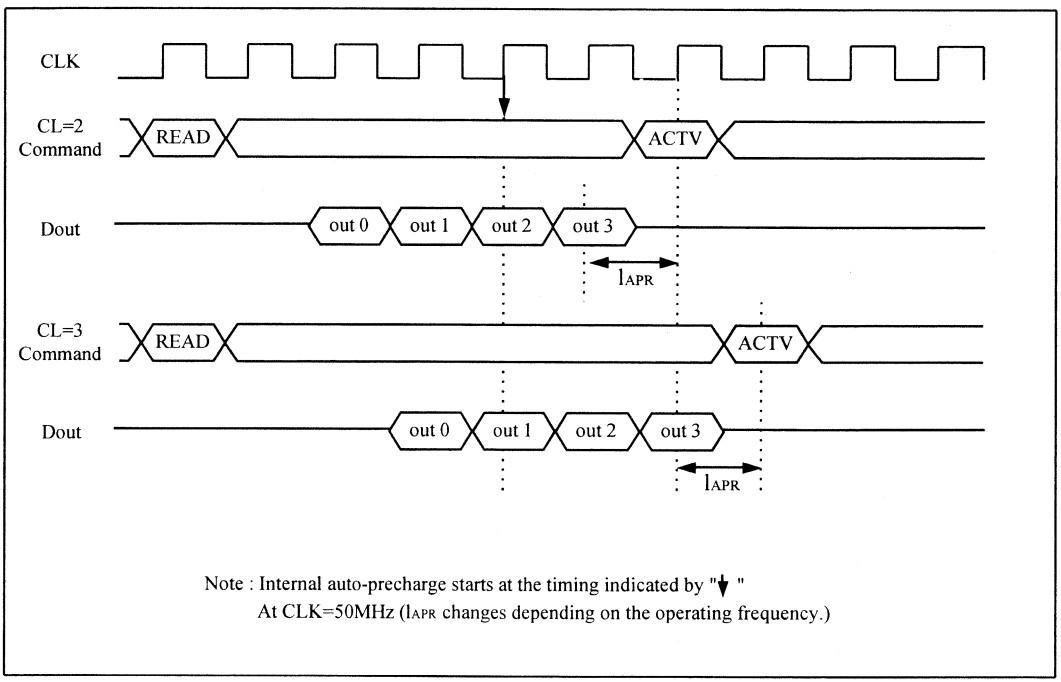


Auto Precharge

• **Read with auto-precharge:** In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by t_{APR} is required before execution of the next command.

$\overline{CAS}$ Latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output

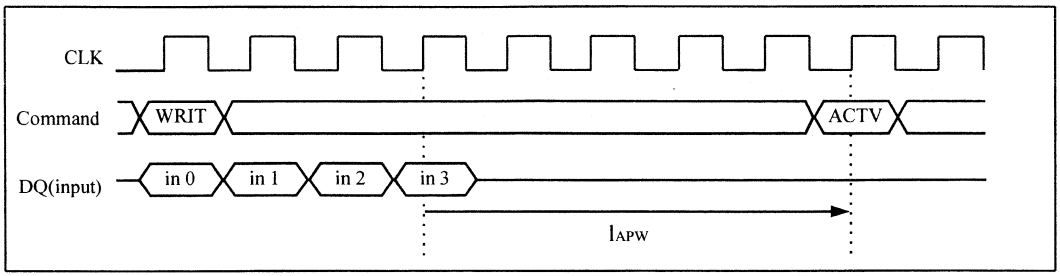
Burst Read with Auto-precharge



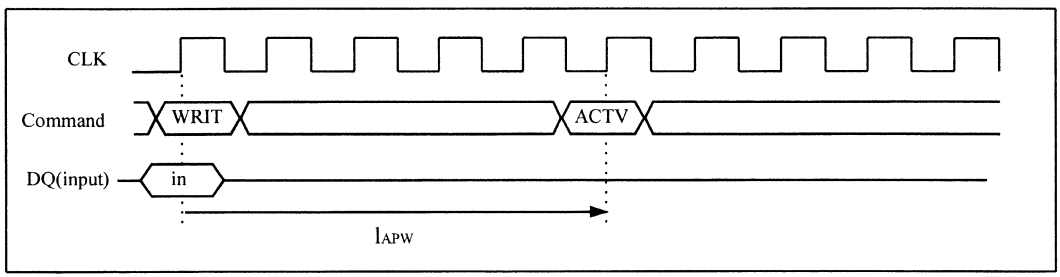
Note : Internal auto-precharge starts at the timing indicated by "↓ "
At CLK=50MHz (t_{APR} changes depending on the operating frequency.)

• **Write with auto-precharge:** In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of t_{APW} is required between the final valid data input and input of the next command.

Burst Write (Burst Length = 4)



Single Write



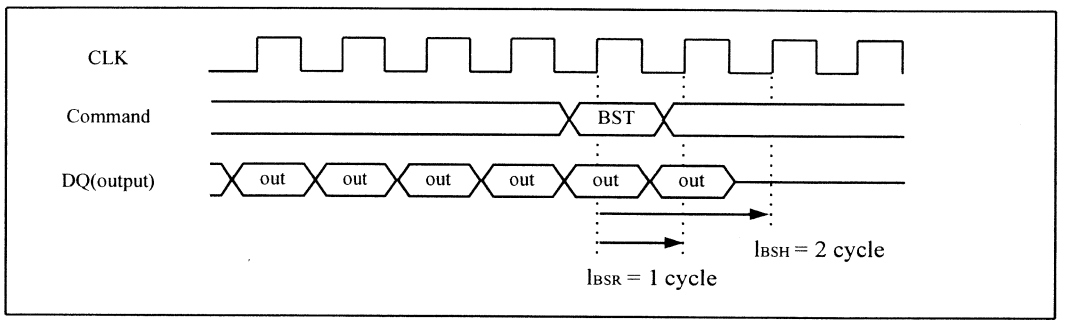
Full-page Burst Stop

• **Burst stop command during burst read:** The burst stop (BST) commnad is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read.

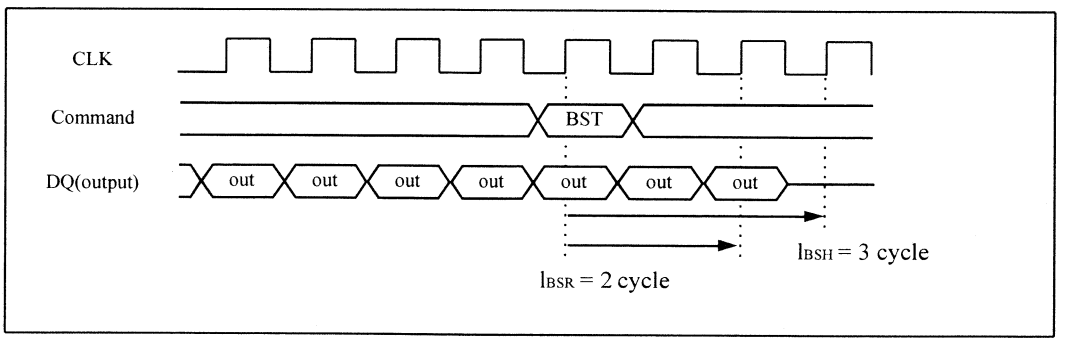
The timing from command input to the last data changes depending on the $\overline{CAS}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is invalid with burst lengths 1, 2, 4, and 8.

$\overline{CAS}$ Latency	BST to valid data	BST to high impedance
2	1	2
3	2	3

$\overline{CAS}$ Latency=2, Burst Length = full page



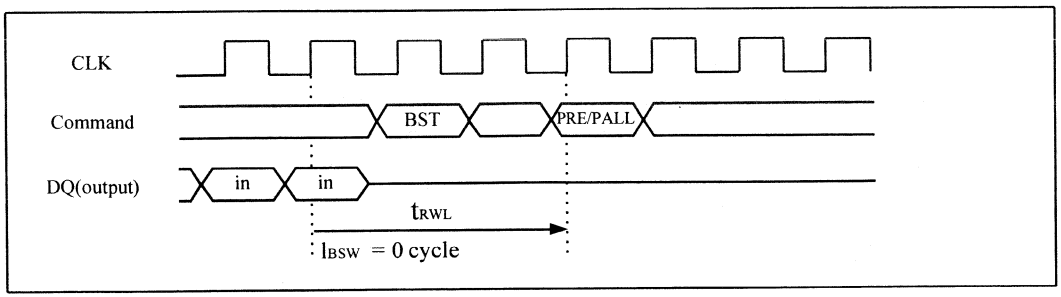
$\overline{CAS}$ Latency = 3, Burst Length = full page



• **Burst stop command at burst write:** The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same cycle as the BST command, and in subsequent cycles.

In addition, the BST command is only valid during full-page burst mode, and is invalid with burst lengths of 1, 2, 4, and 8. And an interval of t_{RWL} is required between the last data-in and the next precharge command.

Burst Length = full page



Command Intervals

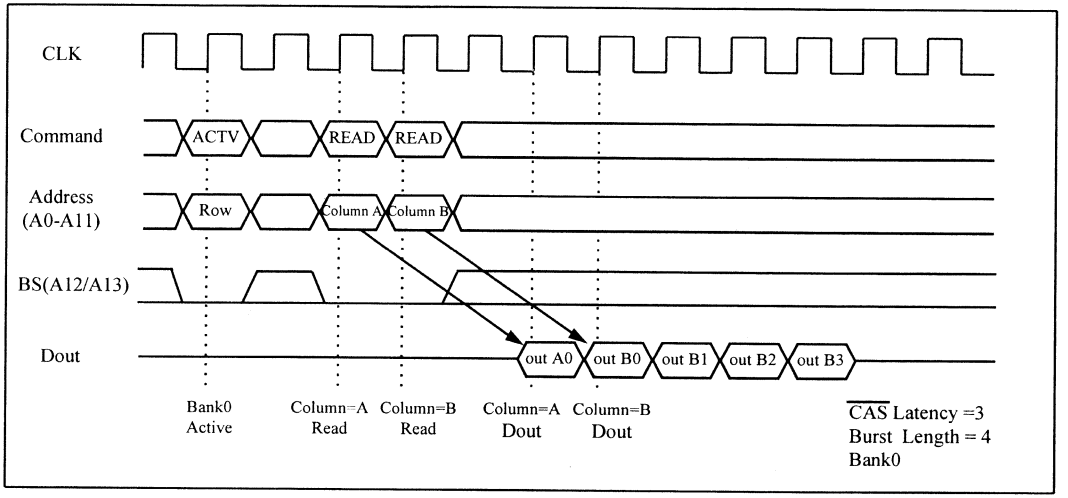
• Read command to Read command interval:

1. Same bank, same ROW address:

When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 cycle.

Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (Same Row Address in Same Bank)



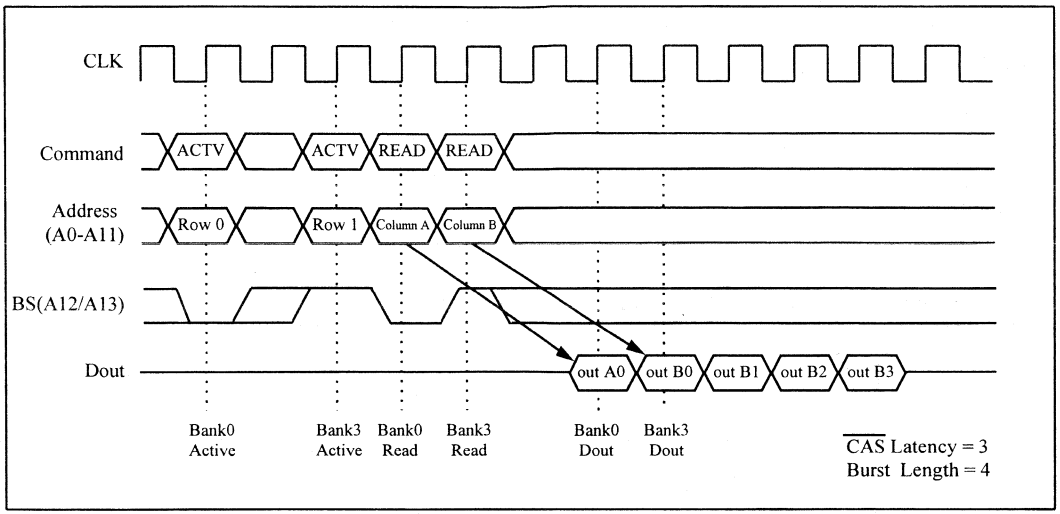
2. Same bank, different ROW address:

When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to seperate the two read commands with a precharge command and a bank-active command.

3. Different bank:

When the bank changes, the second read can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (different bank)



Command Intervals

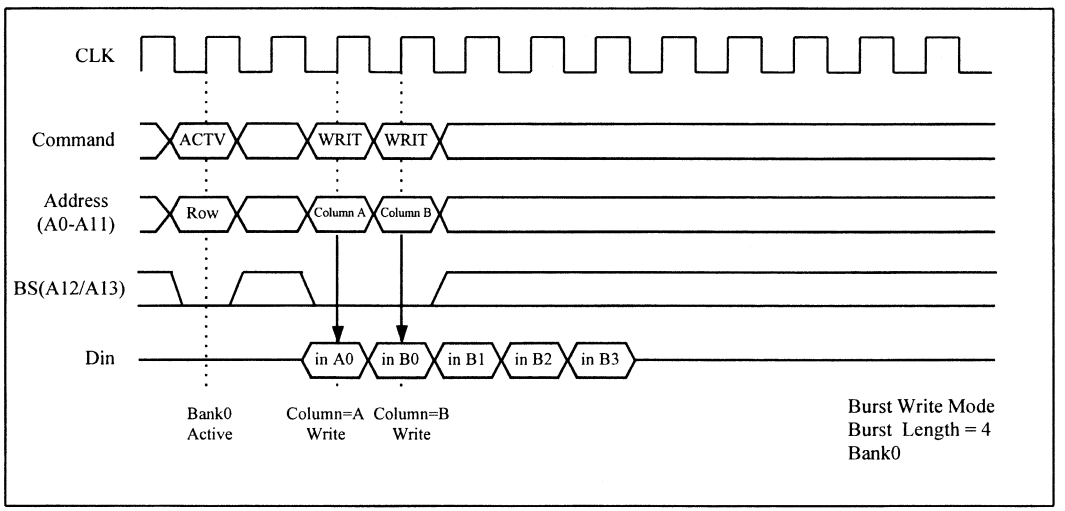
- **Write command to Write command interval:**

1. Same bank, same ROW address:

When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 cycle.

In the case of burst writes, the second write command has priority.

WRITE to WRITE Command Interval (same ROW address in same bank)



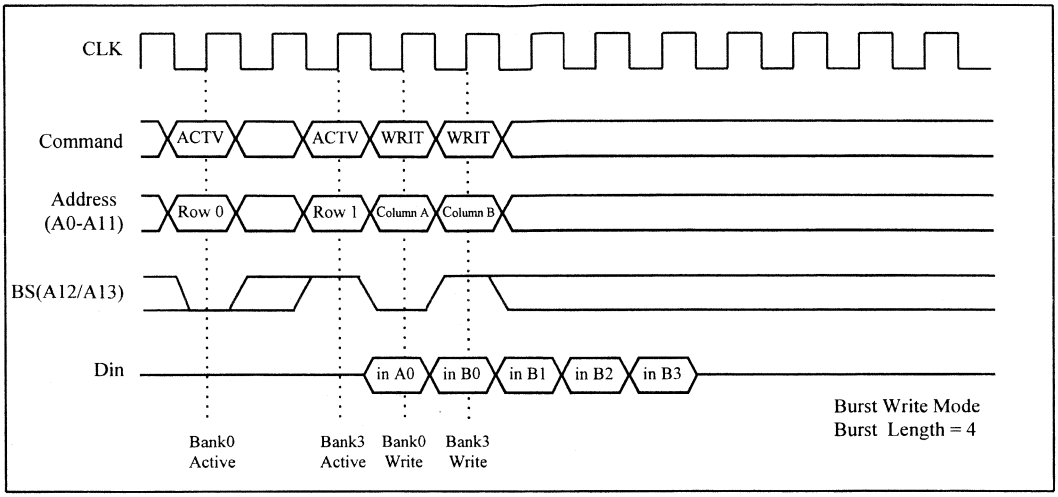
2. Same bank, different ROW address:

When the ROW address changes, consecutive read commands cannot be executed; it is necessary to seperate the two write commands with a precharge command and a bank-active command.

3. Different bank:

When the bank changes, the second write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (different bank)

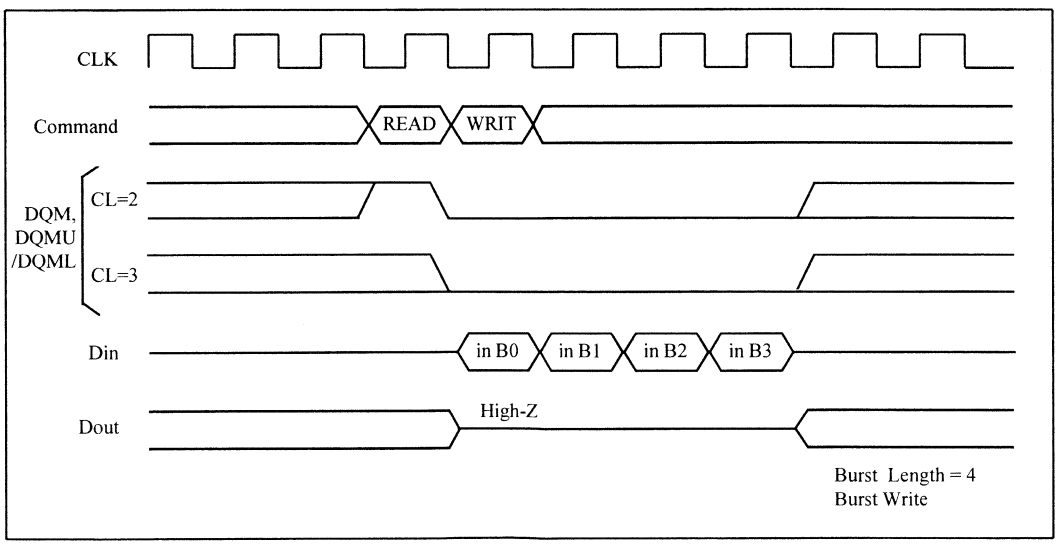


• **Read command to Write command interval:**

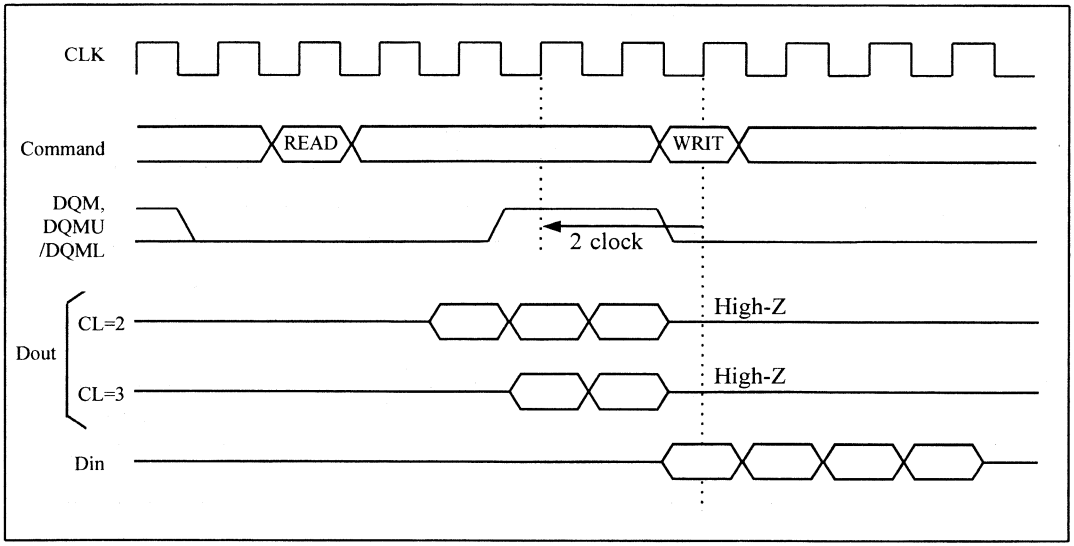
1. **Same bank, same Row address:**

When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 cycle. However, DQM, DQMU/DQML must be set High-Z so that the ouput buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)



READ to WRITE Command Interval (2)



2. Same bank, different ROW address:

When the ROW address changes, consecutive write commands cannot be executed; it is necessary to seperate the two write commands with a precharge command or a bank-active command.

3. Different bank:

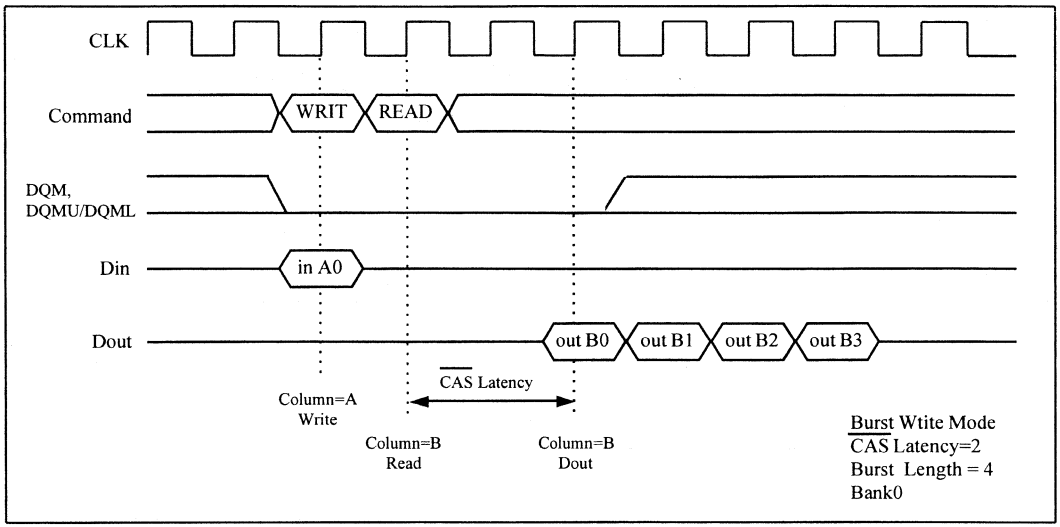
When the bank changes, the write can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, DQM, DQMU/DQML must be set High so that the output buffer becomes High-Z before data input.

• **Write Command to Read Command Interval:**

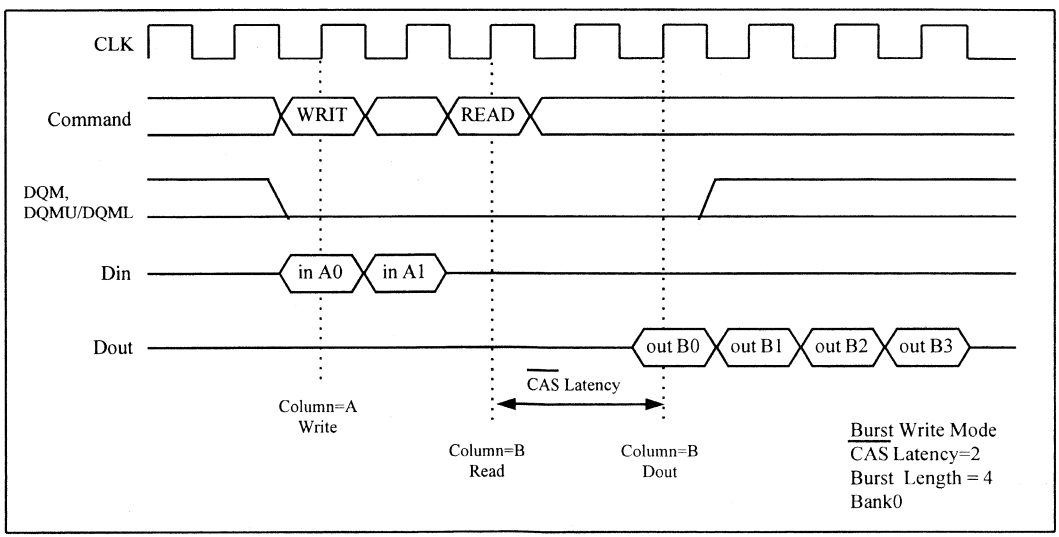
1. **Same bank, same Row address:** When the read command is executed at the same ROW address of the same bank as the preceding write command, the write command can be performed after an interval of no less than 1 cycle.

However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)



WRITE to READ Command Interval (2)



2. **Same bank, different ROW address:** When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

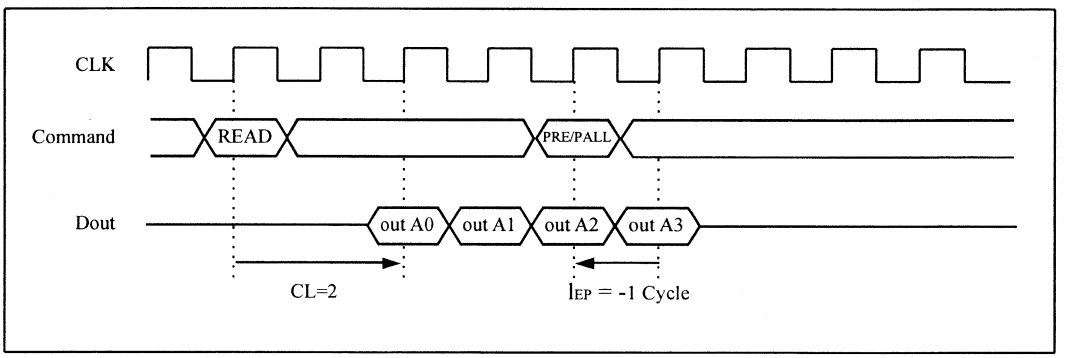
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed(as in the case of the same bank and the same address).

• Read command to Precharge interval (same bank): When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one cycle. However, since the output buffer then becomes High-Z after the cycles defined by l_{HZP}, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read.

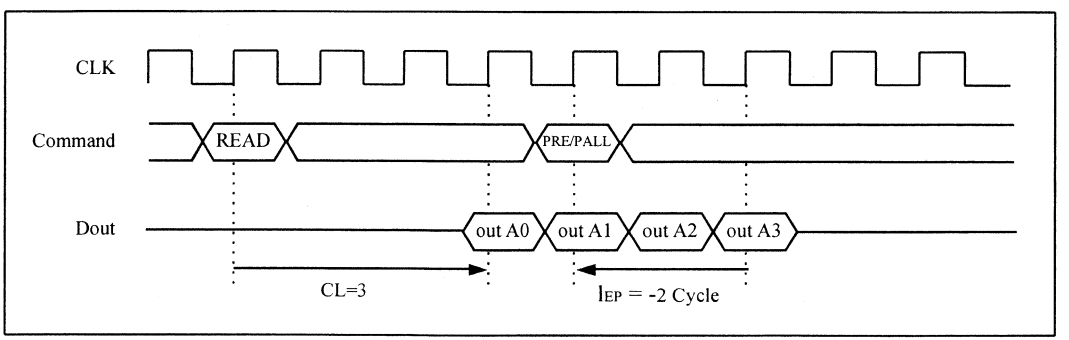
To read all data by burst read, the cycles defined by l_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank) : To output all data

$\overline{CAS}$ Latency = 2, Burst Length = 4

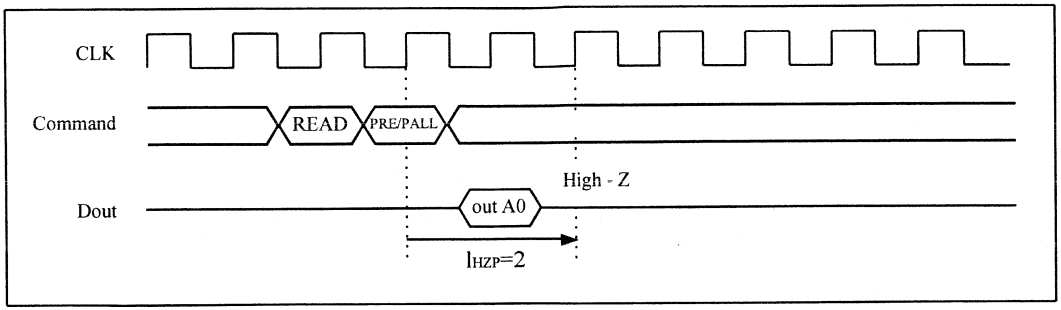


$\overline{CAS}$ Latency = 3, Burst Length = 4

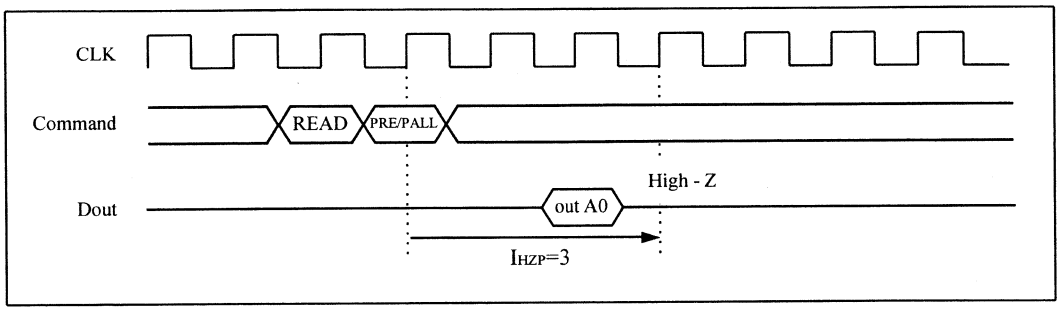


READ to PRECHARGE Command Interval (same bank) : To stop output data

$\overline{CAS}$ Latency = 2, Burst Length = 1, 2, 4, 8

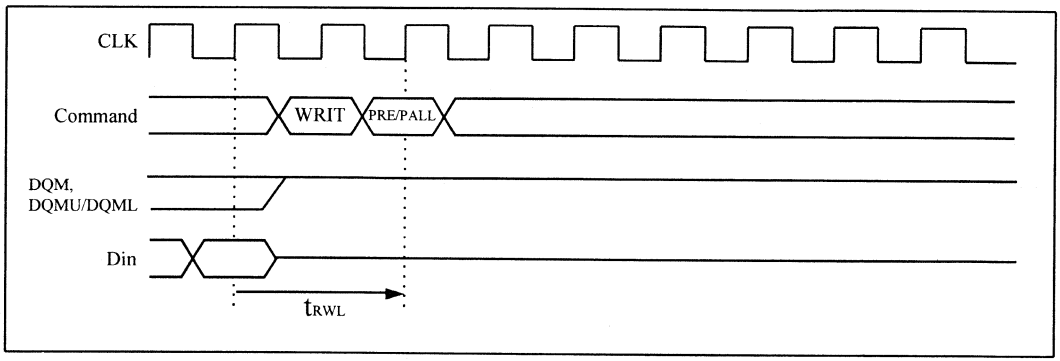


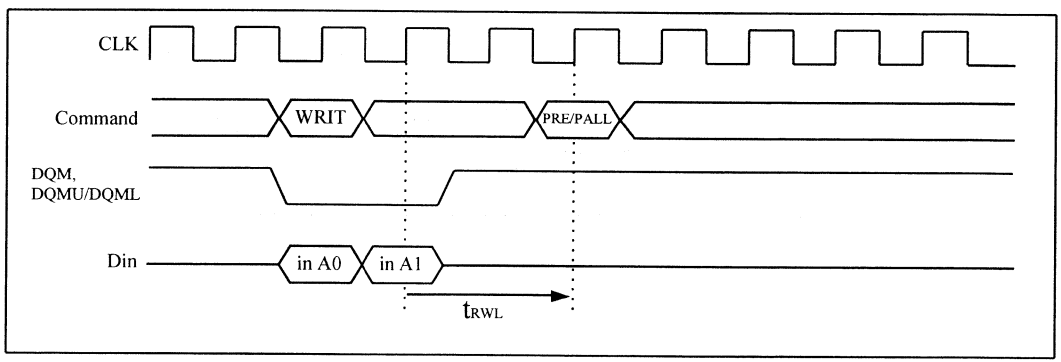
$\overline{CAS}$ Latency = 3, Burst Length = 1, 2, 4, 8



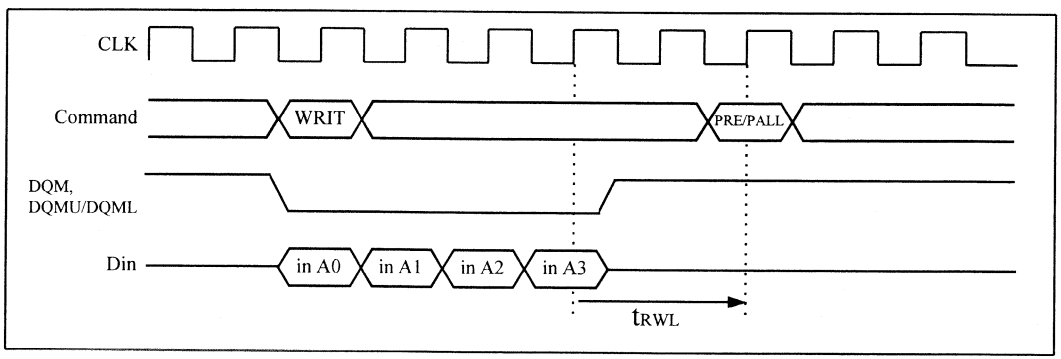
• **Write Command to Precharge Command Interval (same bank):** When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 cycle. However, if the burst write operation is unfinished, the input data must be masked by means of DQM, DQMU/DQML for assurance of the cycle defined by t_{RWL}.

Burst Length = 4 (To stop write operation)





Burst Length = 4 (To write all data)

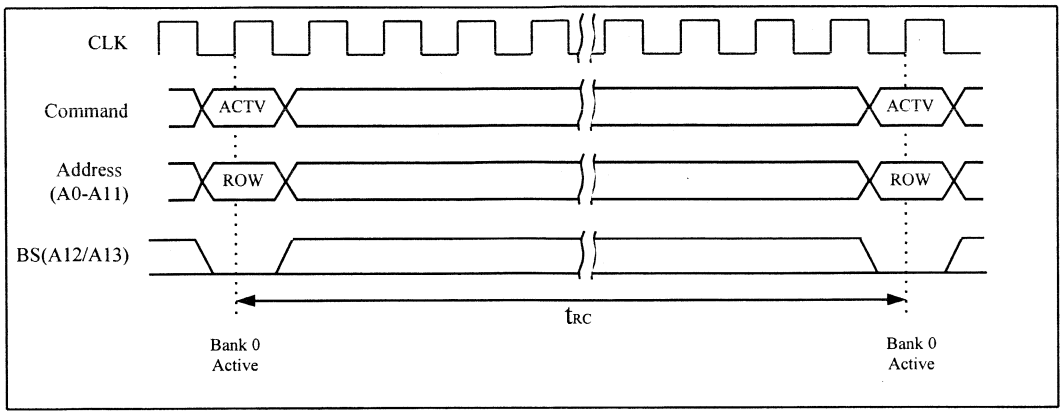


• **Bank Active Command Interval**

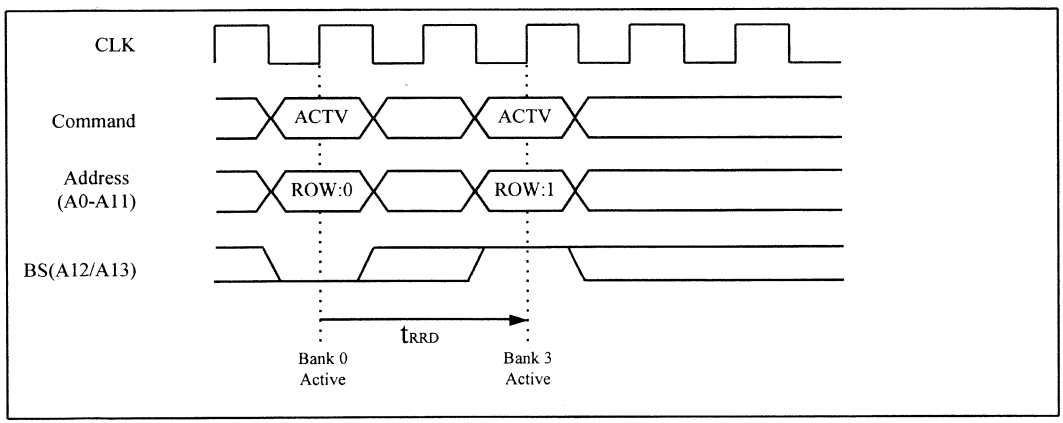
1. **Same bank:** The interval between the two bank-active commands must be no less than t_{RC}.

2. **In the case of different bank-active commands:** The interval between the bank-active commands must be no less than t_{RRD}.

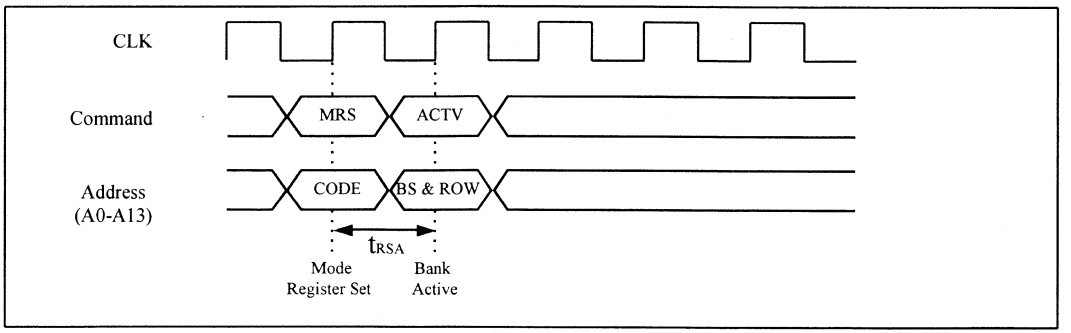
Bank Active to Bank Active Command Interval for Same Bank



Bank Active to Bank Active for different bank



• **Mode Register Set to Bank-Active Command Interval :** The interval between setting the mode register and executing a bank-active command must be no less than t_{RSA}.



DQM Control (GM72V661641CT)

The DQMU and DQML mask the upper and lower bytes of DQ data, respectively. The timing of DQMU/DQML is different during reading and writing.

• **Reading:** When data is read, the output buffer can be controlled by DQMU/DQML. By setting DQMU/DQML to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMU/DQML to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMU/DQML during reading is 2.

• **Writing:** Input data can be masked by DQMU/DQML. By setting DQMU/DQML to Low, data can be written. In addition, when DQMU/DQML is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMU/DQML during writing is 0.

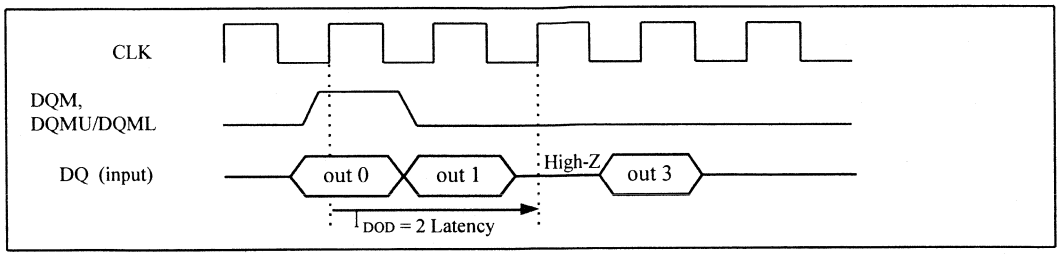
DQM Control (GM72V66841CT, M72V66441CT)

The DQM mask DQ data. The timing of DQM is different during reading and writing.

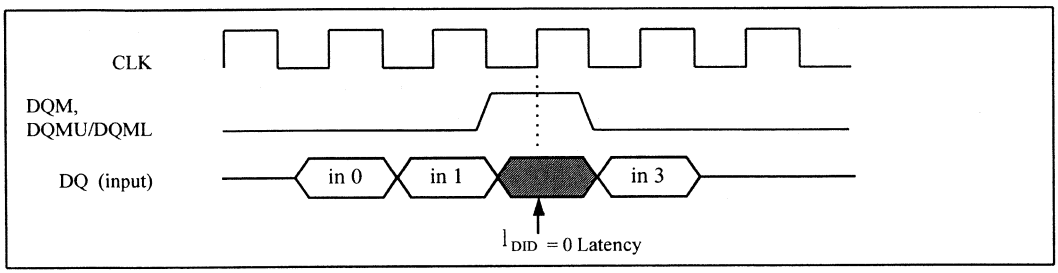
• **Reading:** When data is read, the output buffer can be controlled by DQM. By setting DQM to Low, the output buffer becomes Low-Z, enabling data output. By setting DQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQM during reading is 2.

• **Writing:** Input data can be masked by DQM. By setting DQM to Low, data can be written. In addition, when DQM is set to High, the corresponding data is not written, and the previous data is held. The latency of DQM during writing is 0.

Reading



Writing



Refresh

• Auto refresh:

All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4,096 cycles/64ms. (4,096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

• Self refresh:

After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. If you use distributed auto-refresh mode with 15.6 s interval in normal read/write cycle, auto-refresh should be executed within 15.6 s immediately after exiting from and before entering into self refresh mode. If you use address refresh or burst auto-refresh mode in normal read/write cycle, 4096 cycles of distributed auto-refresh with 15.6 s interval should be executed within 64 ms immediately after exiting from and before entering into self refresh mode.

Others

• Power down mode:

The synchronous DRAM enters power down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the synchronous DRAM exits from the power down mode, and command input is enabled from the next cycle. In this mode, internal refresh is not performed.

• Clock suspend (Active power down) mode:

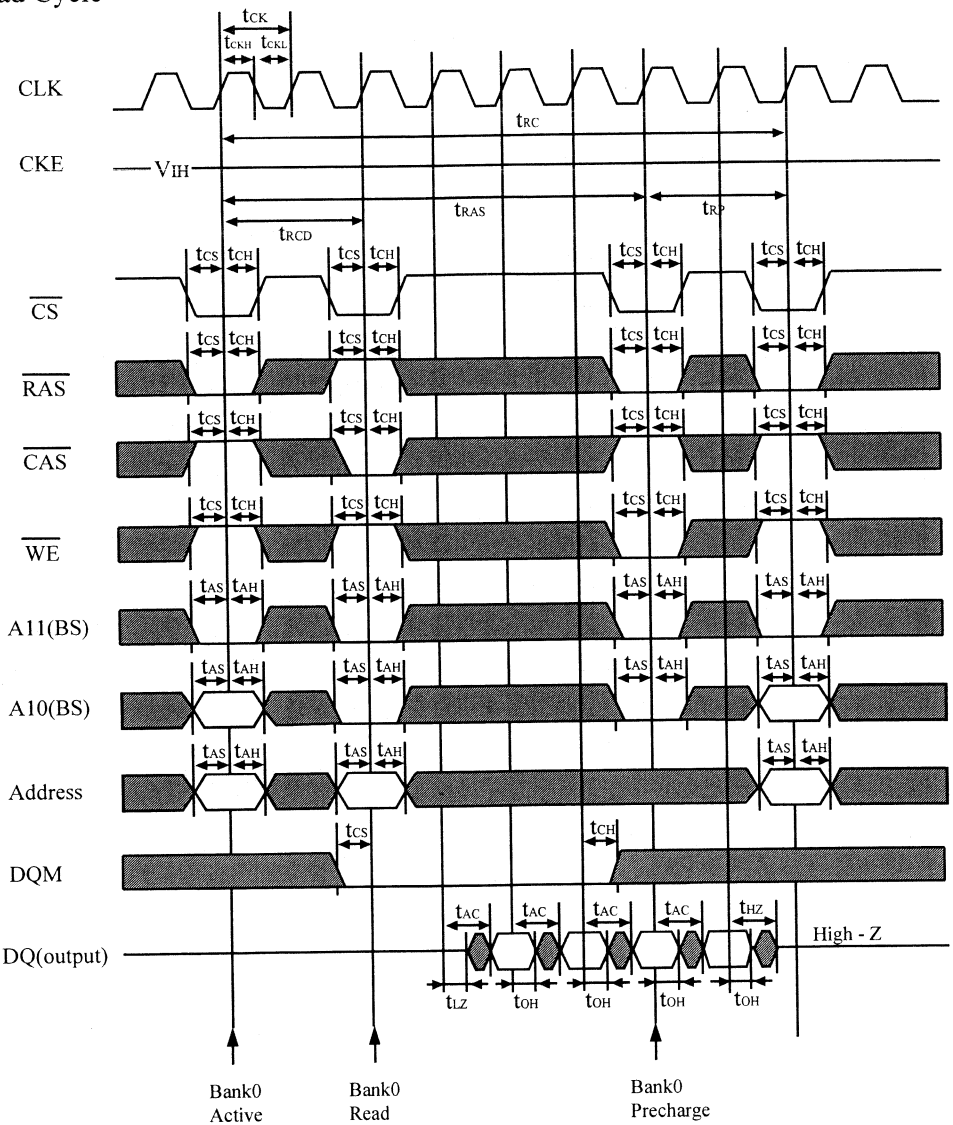
By driving CKE to Low during a bank-active or read/write operation, the synchronous DRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the synchronous DRAM terminates clock suspend mode, and command input is enabled from the next cycle. For details, refer to the "CKE Truth Table".

• Power-up sequence:

During power-up sequence, the DQM and the CKE must be set to High. When 200μs has past after power on, all banks must be precharged using the precharge command. After t_{RP} delay, set 8 or more auto refresh commands. And set the mode register set command to initialize the mode register.

Timing Waveforms

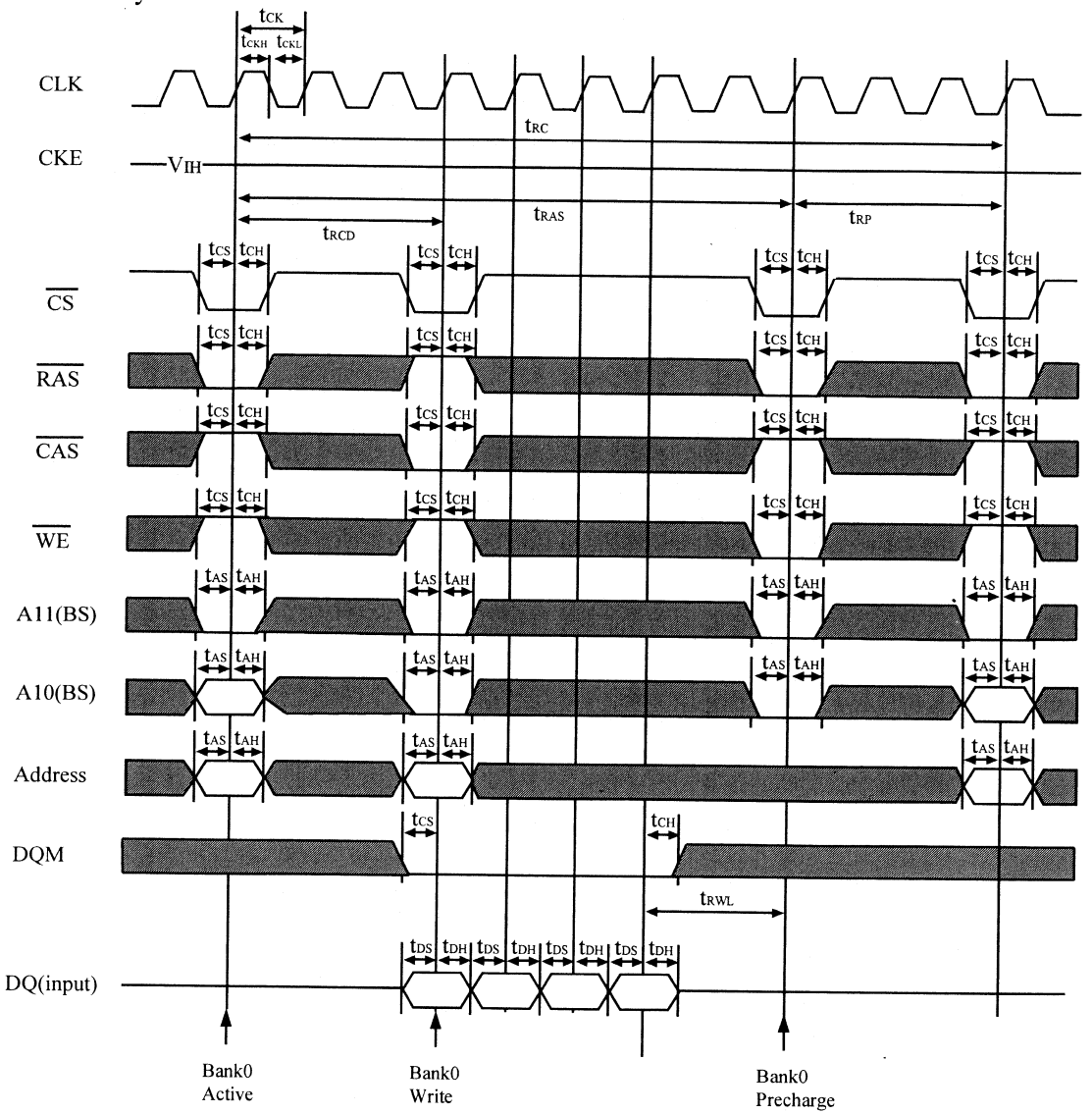
Read Cycle



Burst length = 4
Bank0 Access
▨ = V_{IH} or V_{IL}

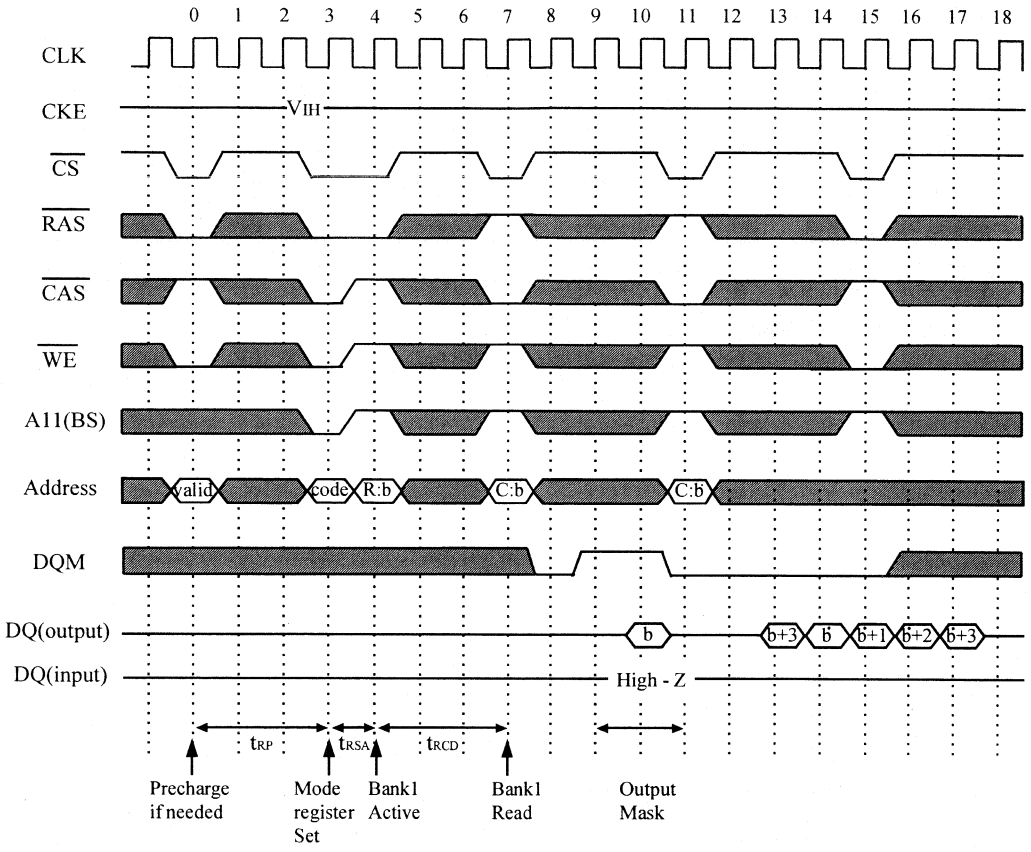
Timing Waveforms

Write Cycle



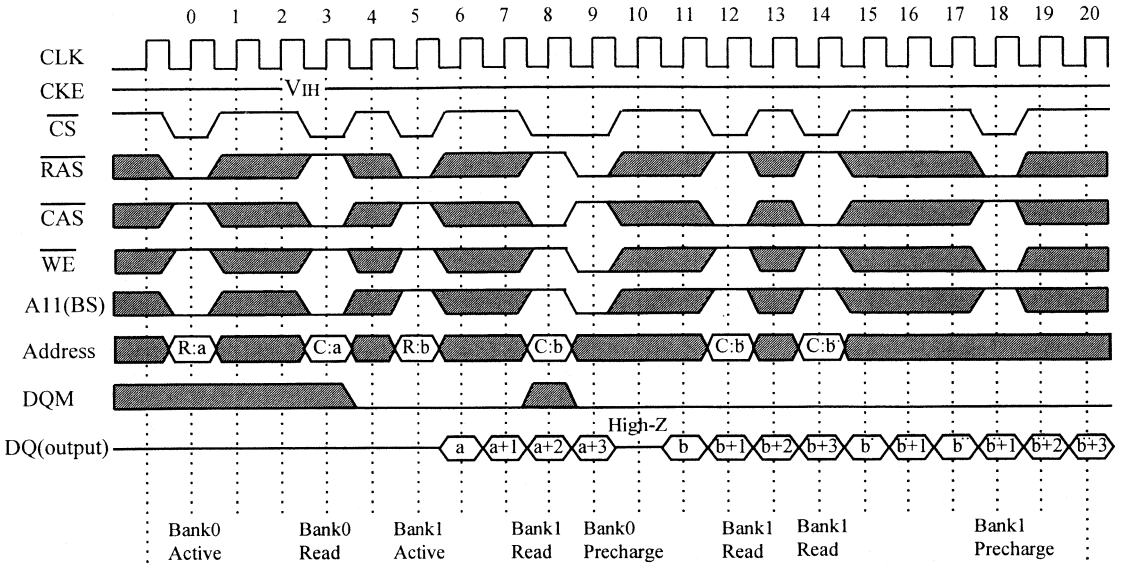
Burst length = 4
Bank0 Access
▨ = V_{IH} or V_{IL}

Mode Register Set Cycle

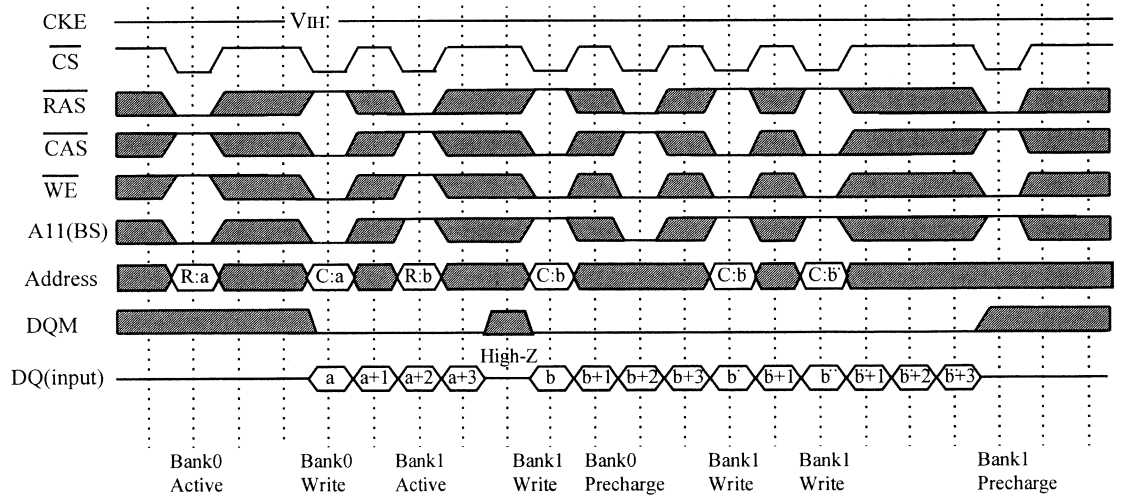


t_{RCD}=3
$\overline{CAS}$ latency=3
Burst length=4
= V_{IH} or V_{IL}

Read Cycle/ Write Cycle

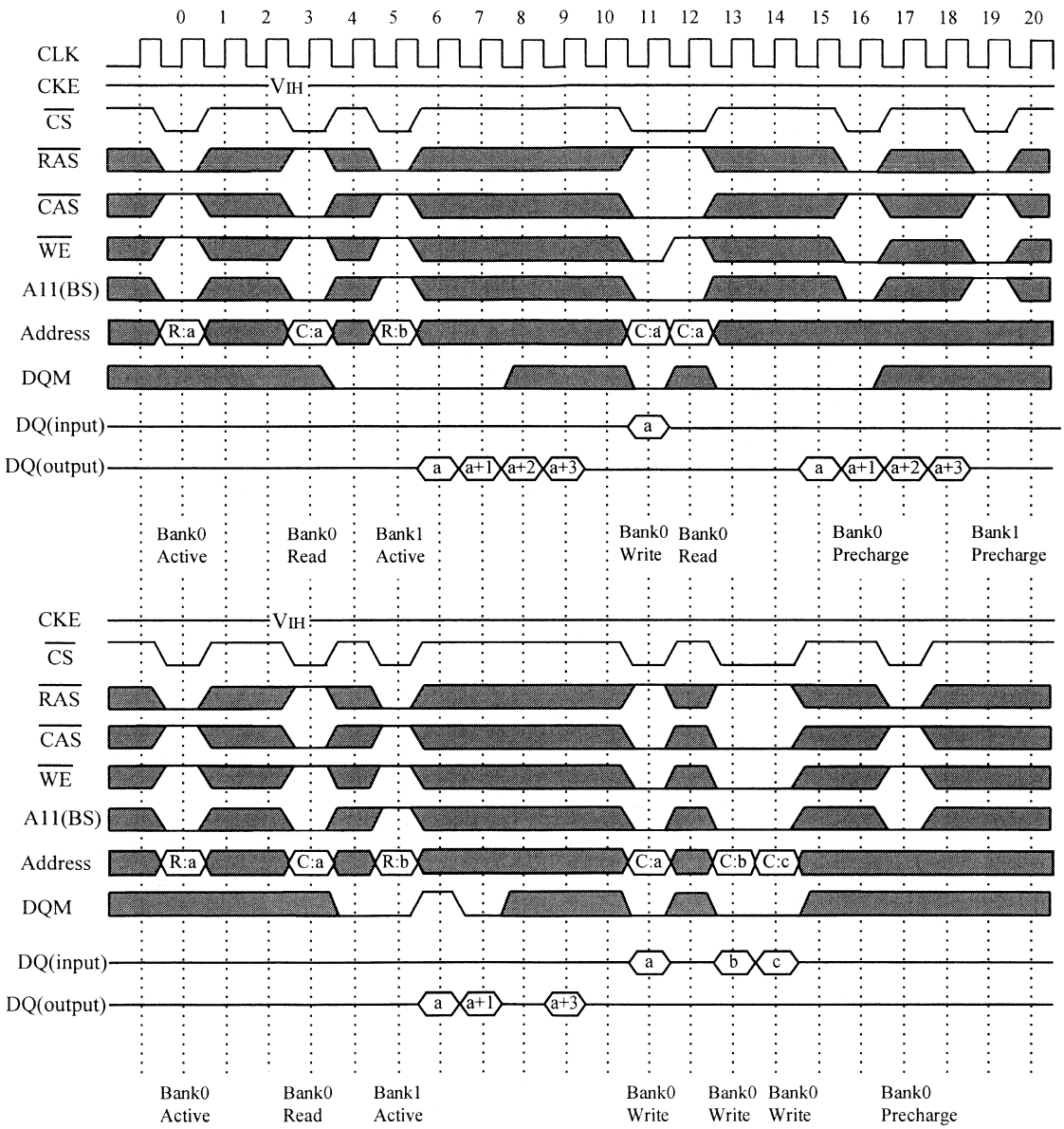


Read cycle
$\overline{RAS}$-$\overline{CAS}$ delay=3
$\overline{CAS}$ latency=3
Burst length=4
▨ = V_{IH} or V_{IL}



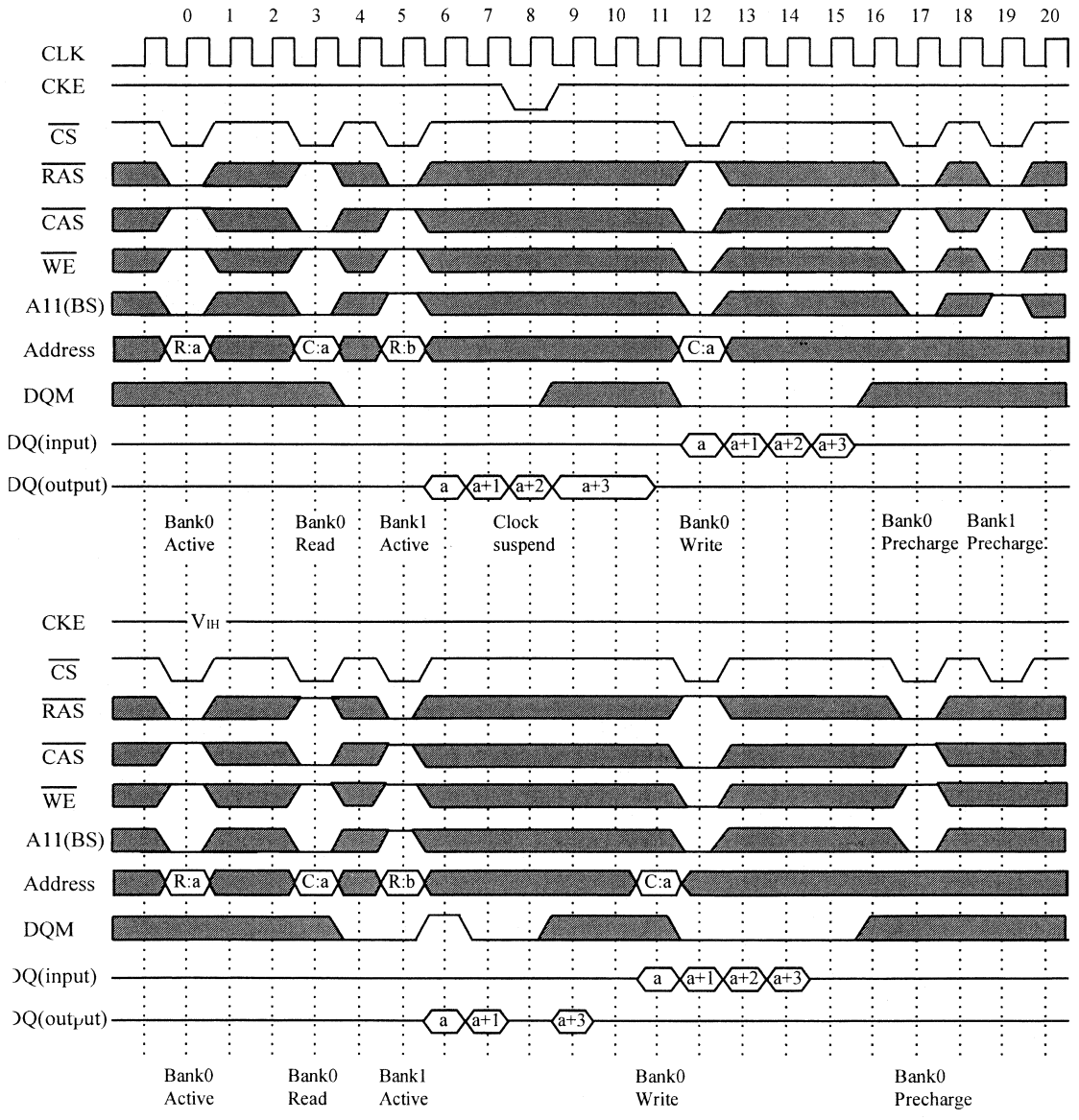
Write cycle
$\overline{RAS}$-$\overline{CAS}$ delay=3
$\overline{CAS}$ latency=3
Burst length=4
▨ = V_{IH} or V_{IL}

Read / Single Write Cycle



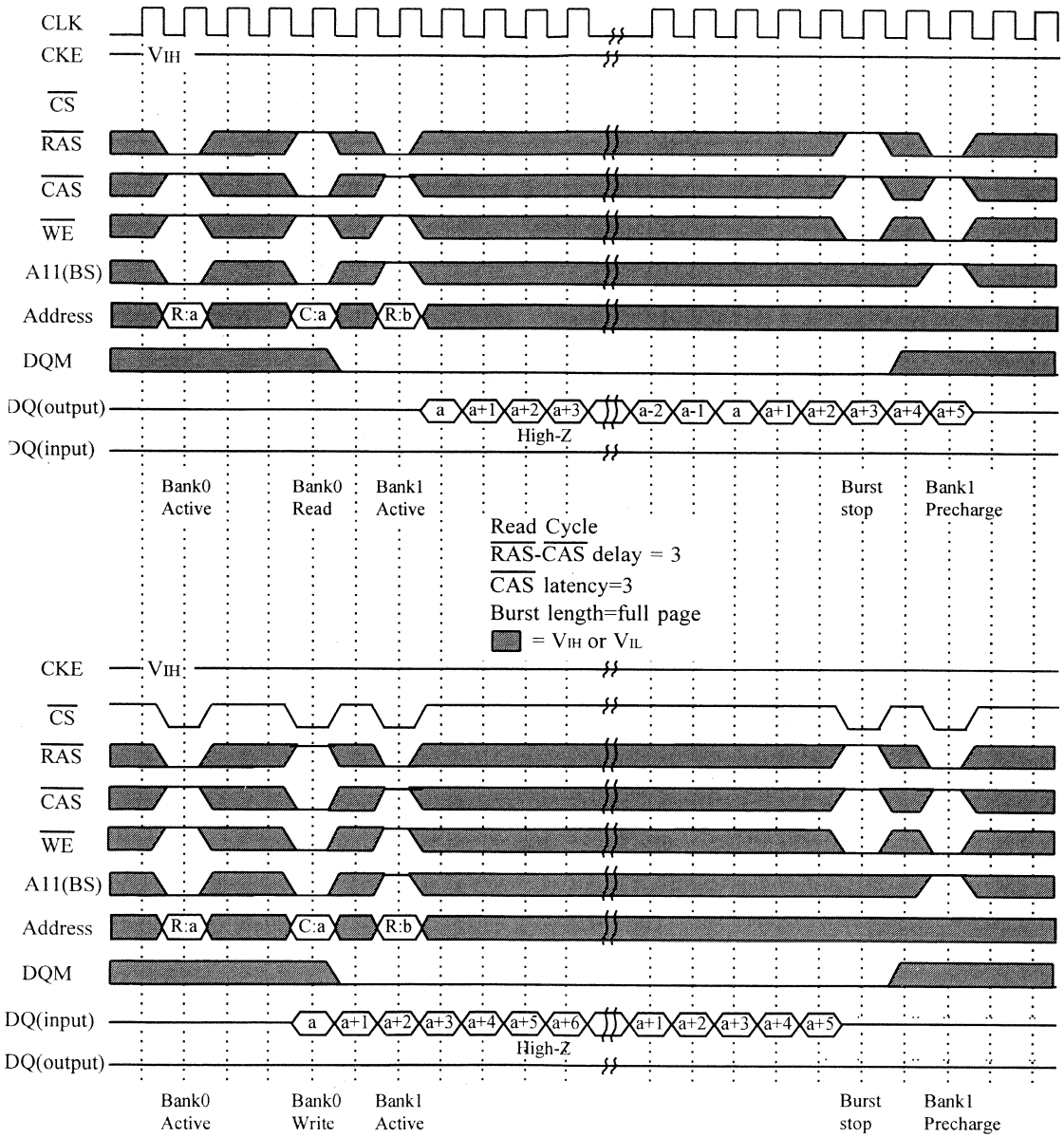
Read/Single write cycle
$\overline{RAS}$-$\overline{CAS}$ delay=3
$\overline{CAS}$ latency=3
Burst length=4
▨ = V_{IH} or V_{IL}

Read / Burst Write Cycle

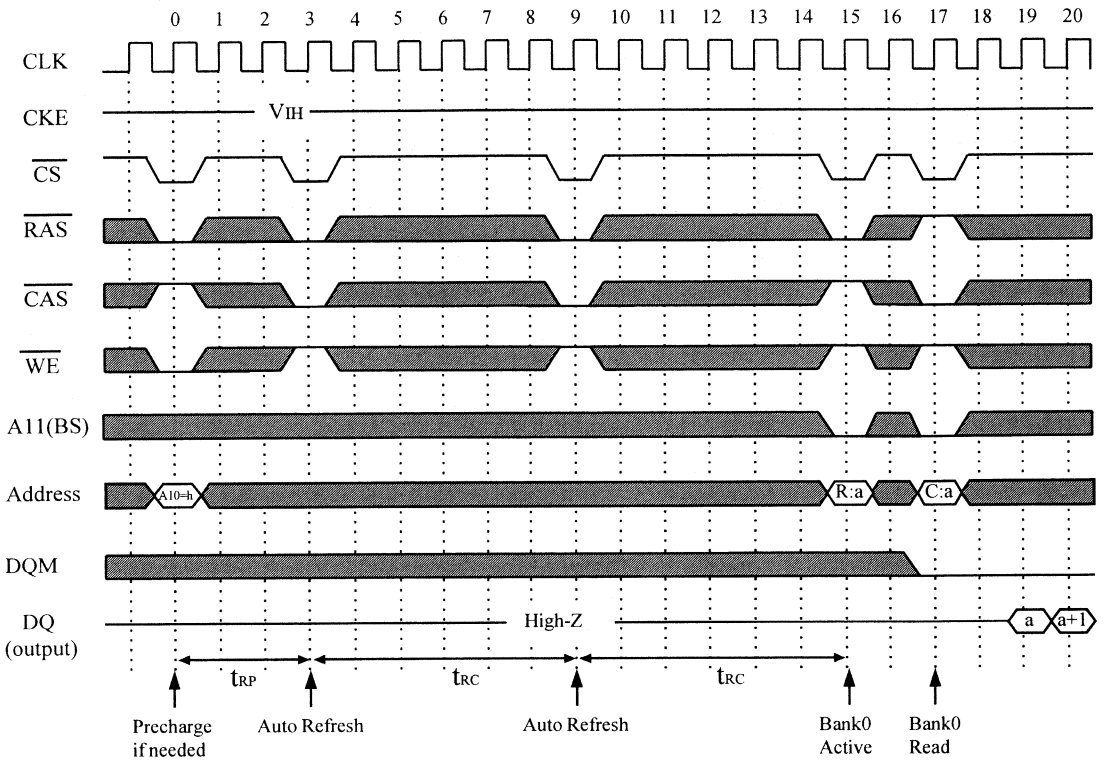


Read/Burst write
$\overline{RAS}$-$\overline{CAS}$ delay=3
$\overline{CAS}$ latency=3
Burst length=4
▨ = V_{IH} or V_{IL}

Full page Read / Write Cycle

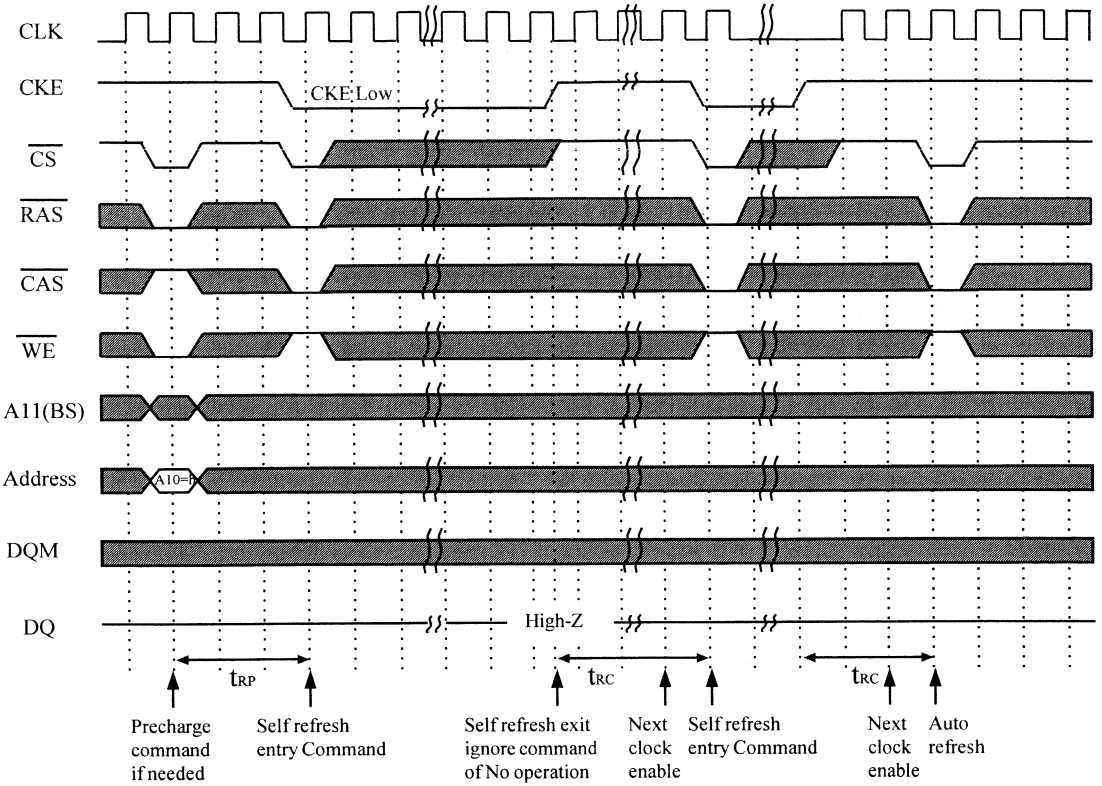


Auto Refresh Cycle



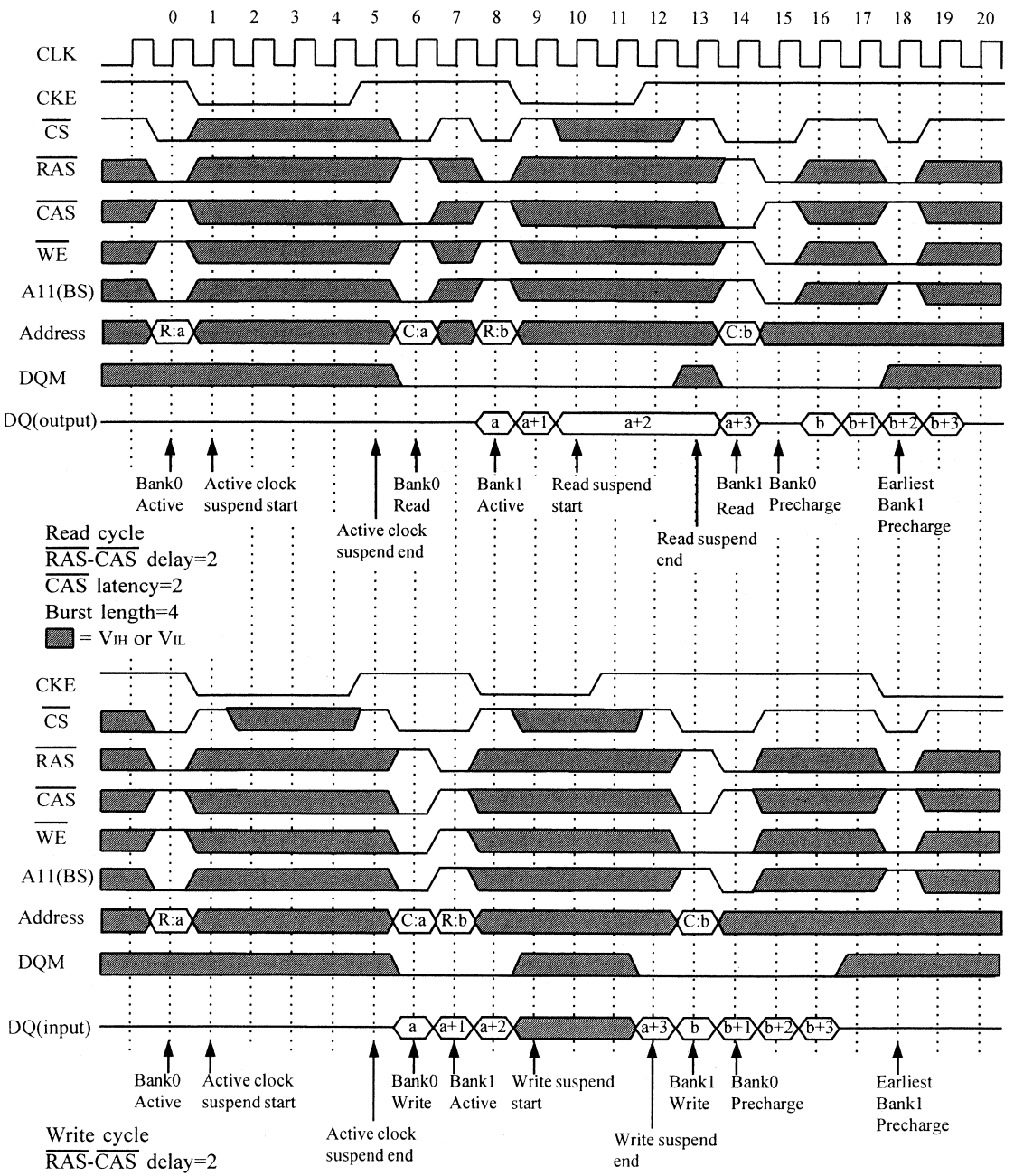
Refresh cycle and
Read cycle
$\overline{RAS}$-$\overline{CAS}$ delay=2
$\overline{CAS}$ latency=2
Burst length=4
▨ = V_{IH} or V_{IL}

Self Refresh Cycle

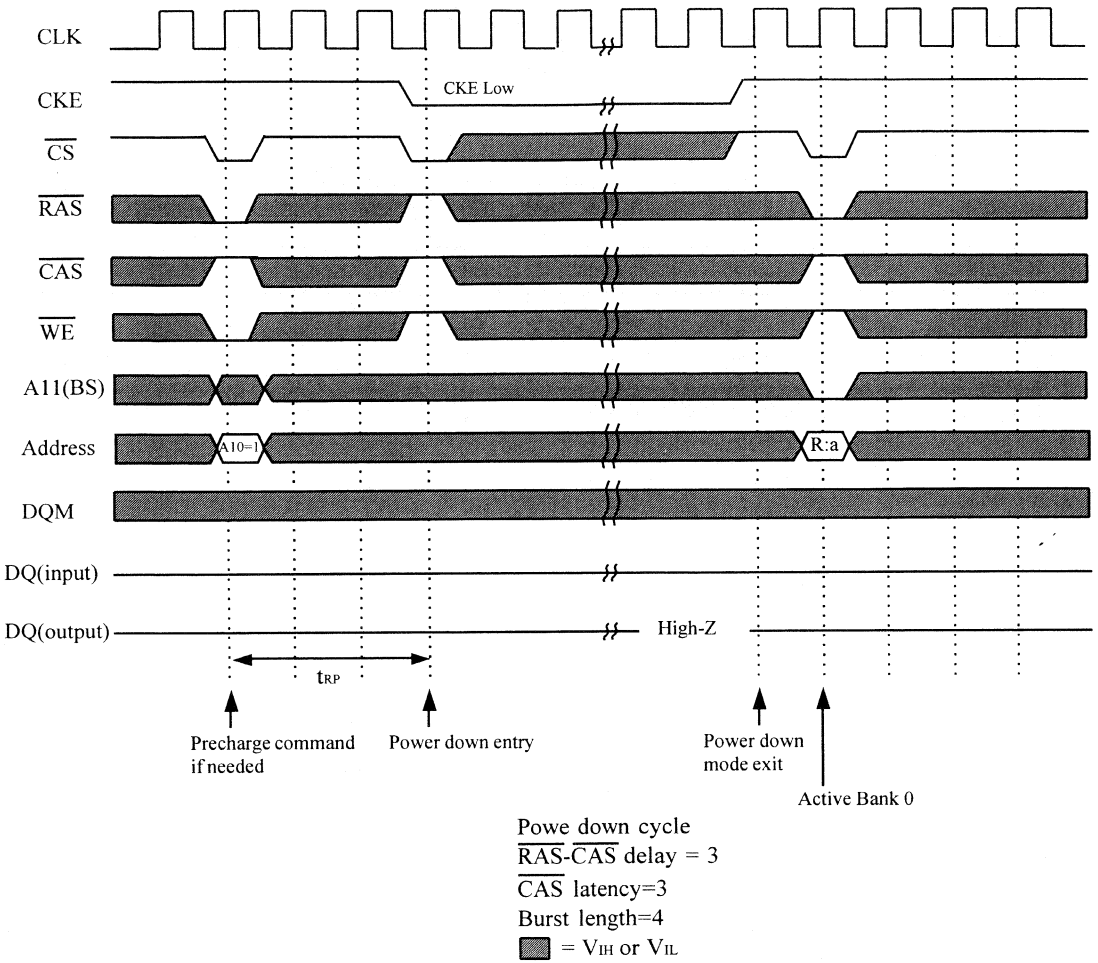


Self refresh Cycle
$\overline{RAS}$-$\overline{CAS}$ delay = 3
$\overline{CAS}$ Latency=3
Burst Length=4
▨ = V_{IH} or V_{IL}

Clock Suspend (Active Power Down) Mode

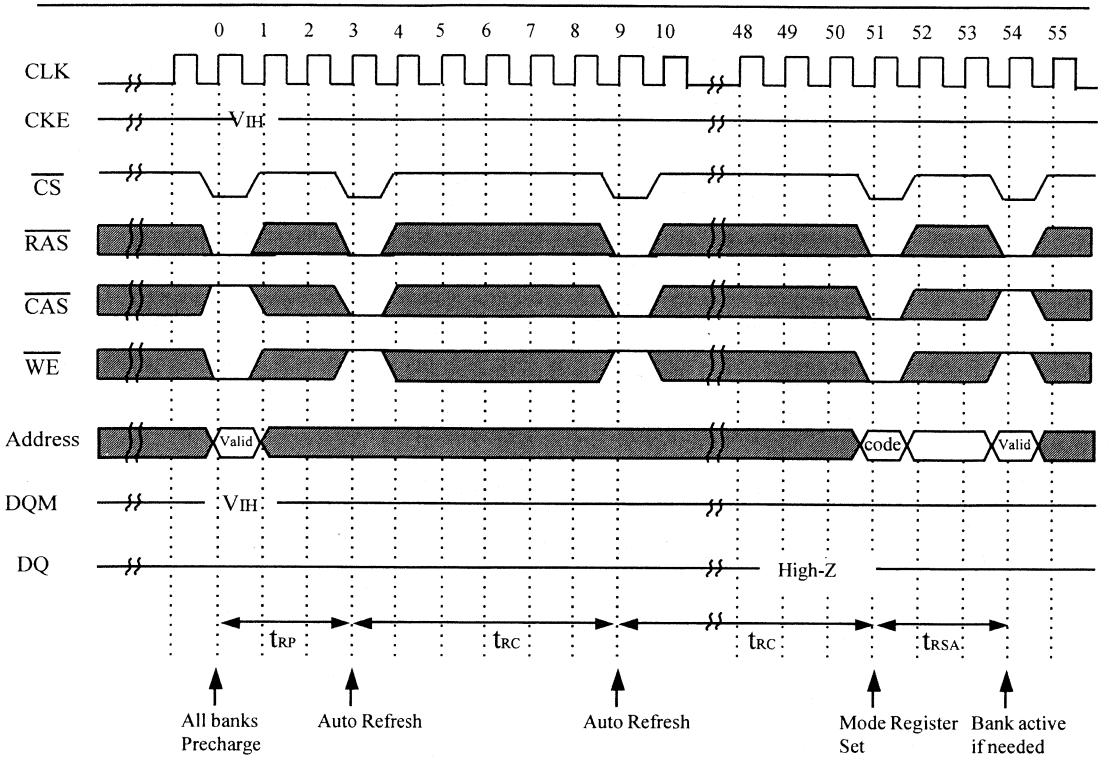


Power Down Mode



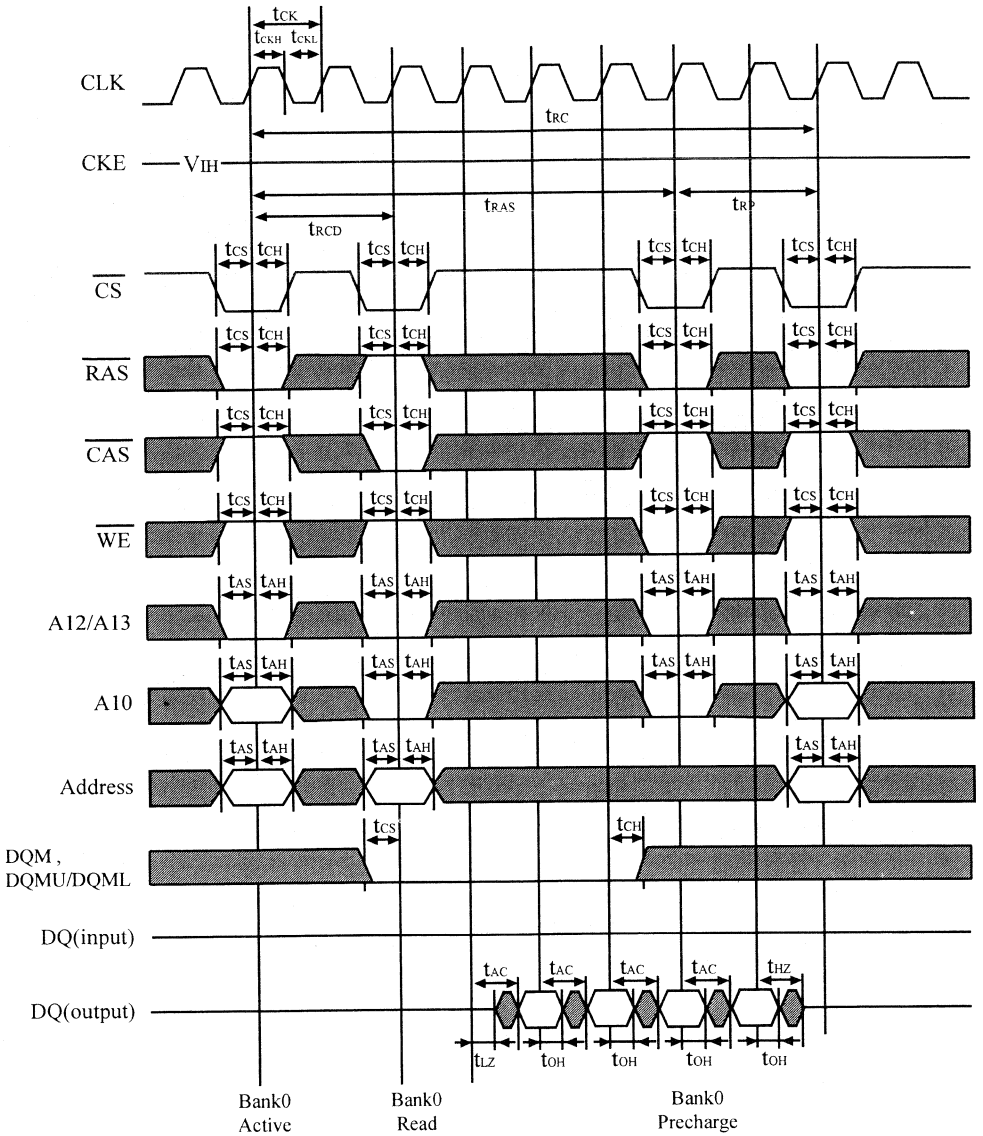
Powe down cycle
RAS-CAS delay = 3
CAS latency=3
Burst length=4
= V_{IH} or V_{IL}

Power Up Sequence



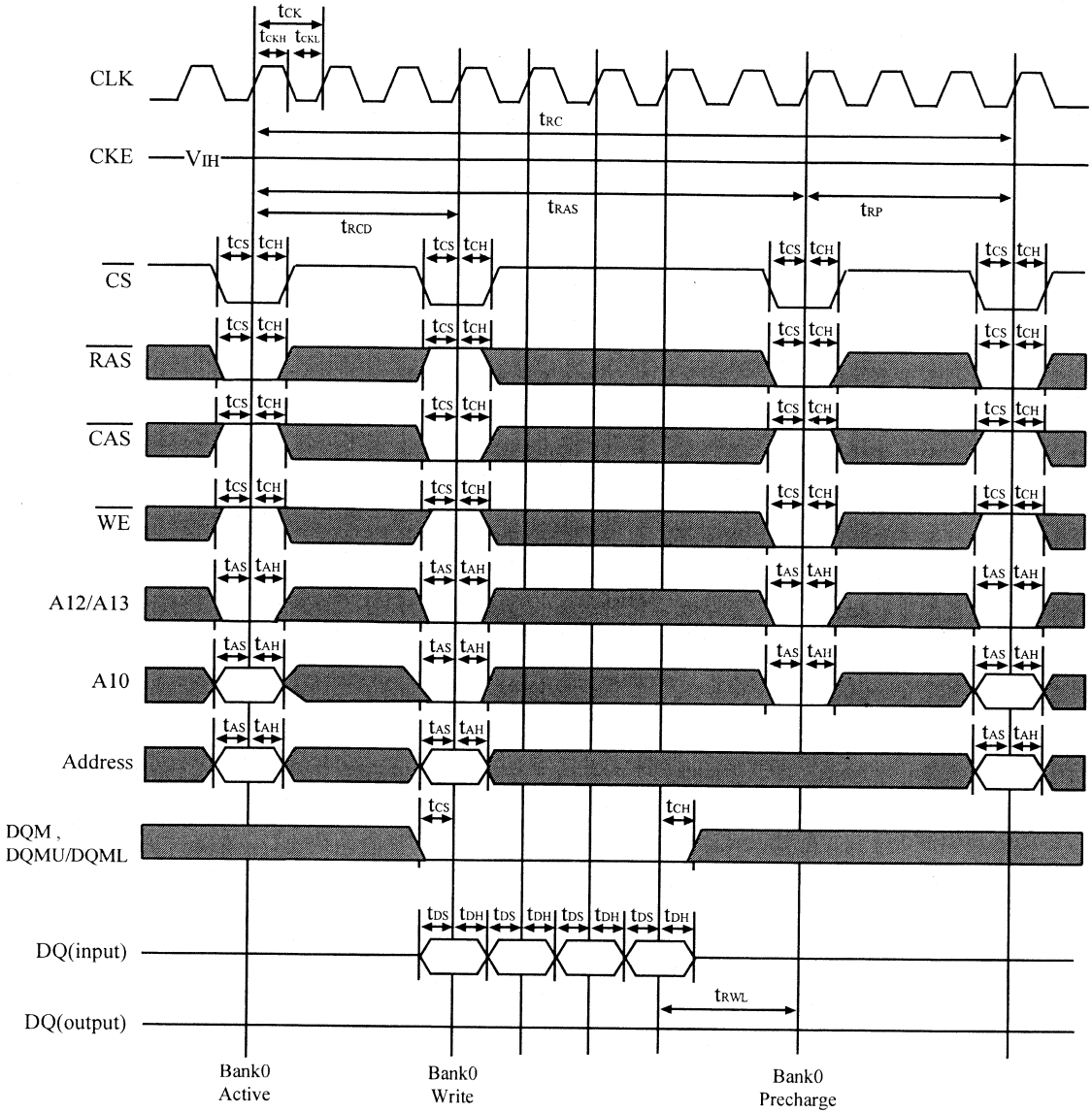
Timing Waveforms

Read Cycle



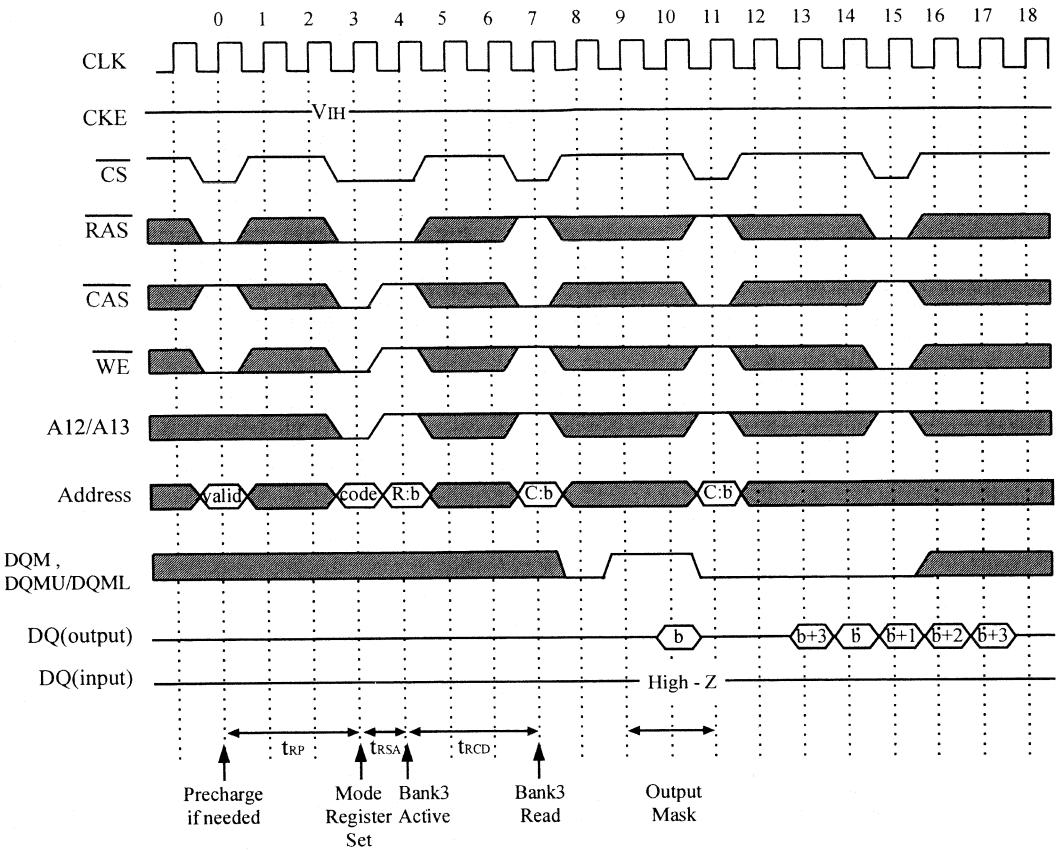
CAS Latency = 2
Burst Length = 4
Bank0 Access
▨ = VIH or VIL

Write Cycle



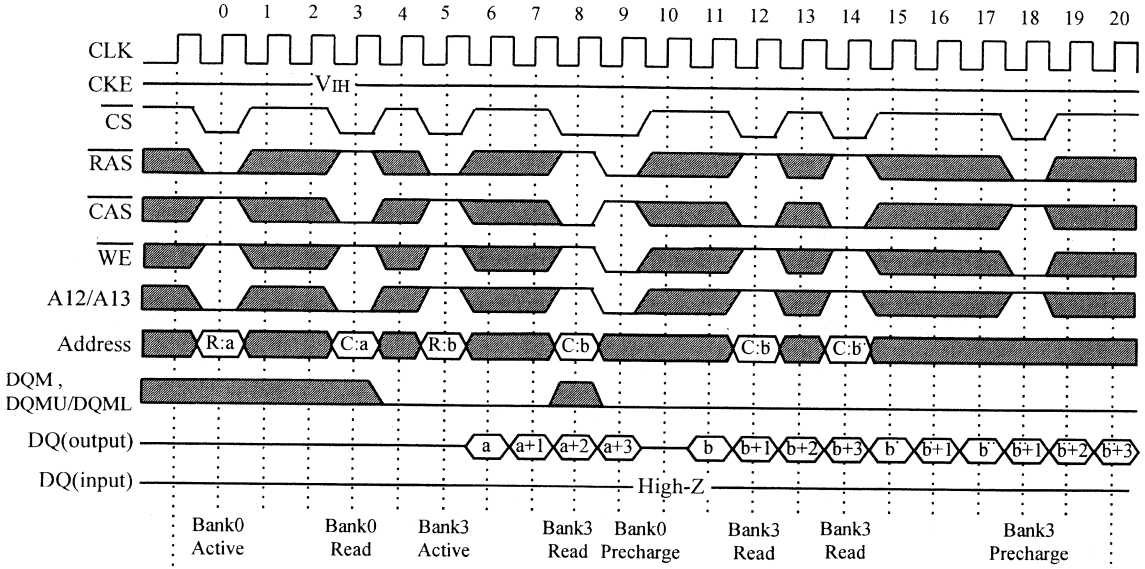
$\overline{\text{CAS}}$ Latency = 2
Burst Length = 4
Bank0 Access
▨ = VIH or VIL

Mode Register Set Cycle

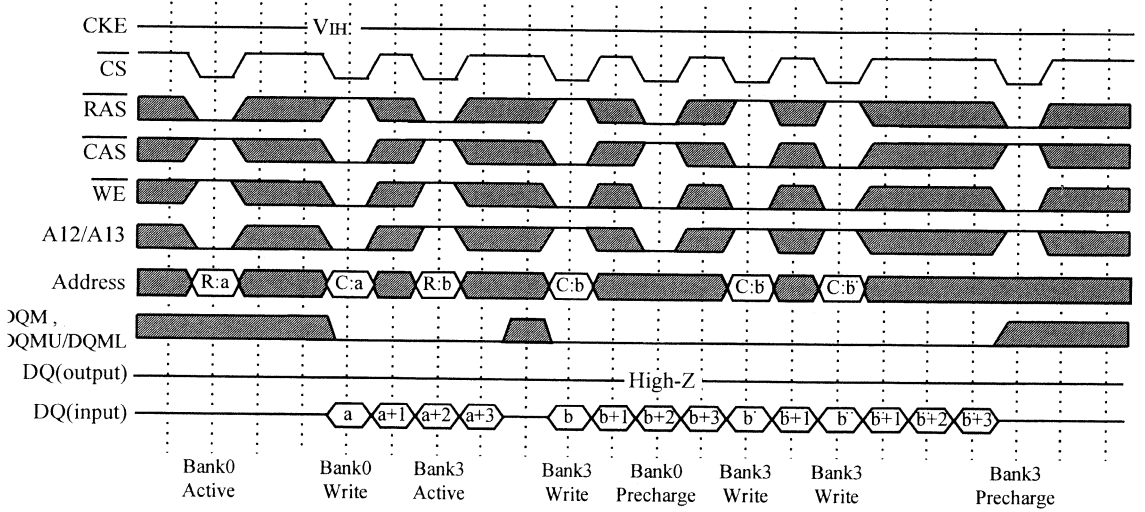


tRCD=3
CAS Latency=3
Burst Length=4
= VIH or VIL

Read Cycle/ Write Cycle

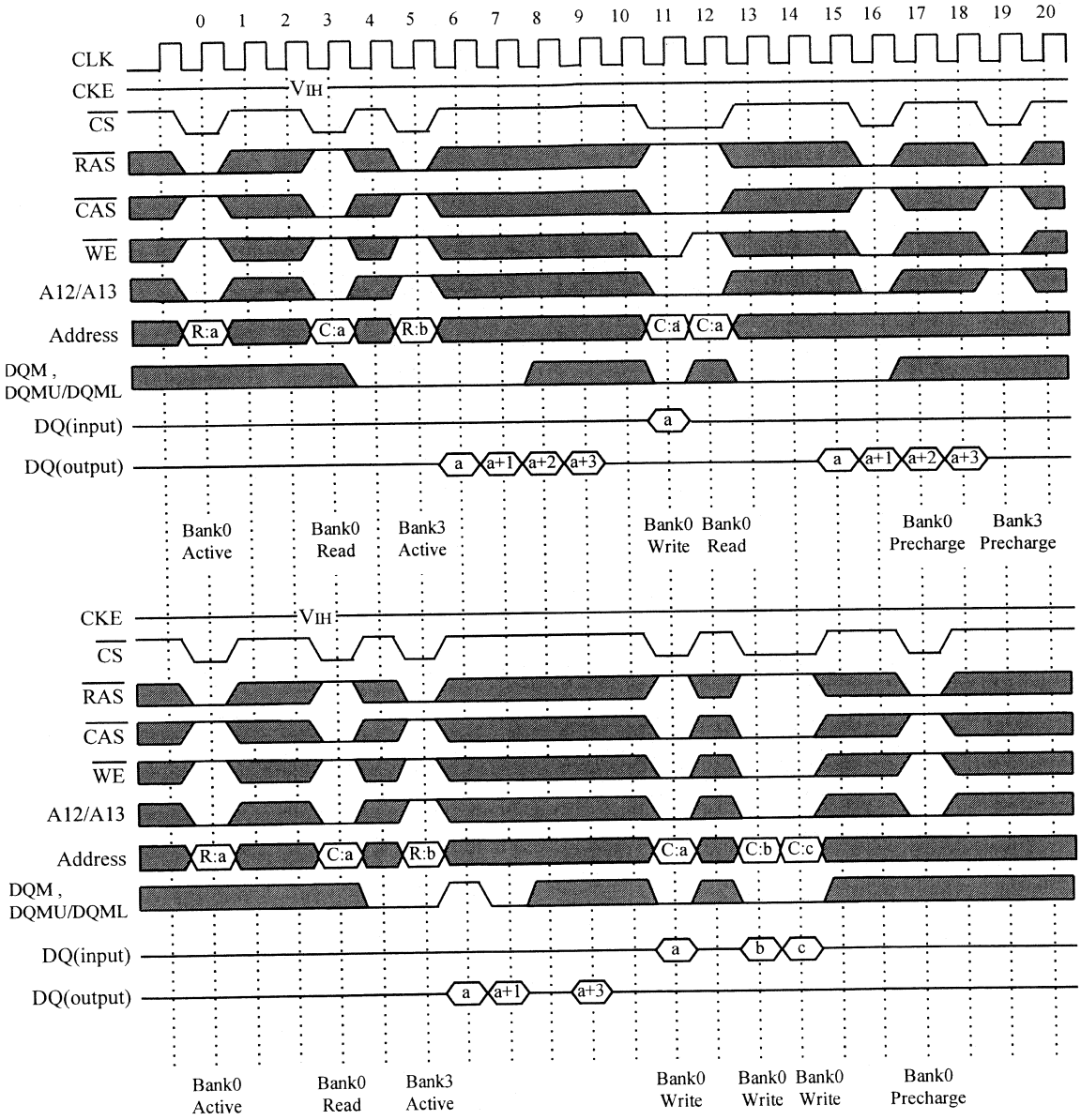


Read Cycle
RAS-CAS Delay=3
CAS Latency=3
Burst Length=4
= VIH or VIL



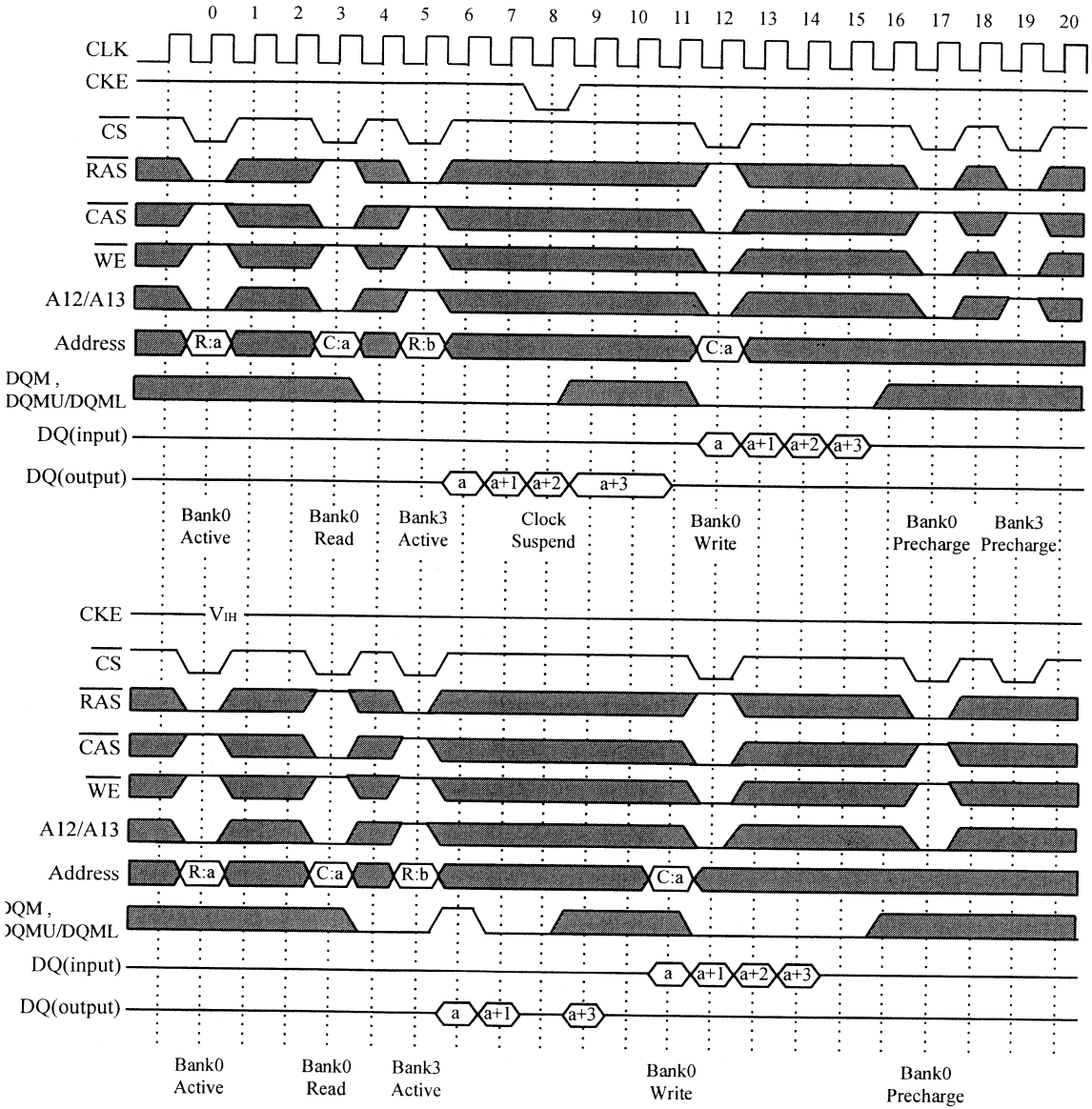
Write Cycle
RAS-CAS Delay=3
CAS Latency=3
Burst Length=4
= VIH or VIL

Read / Single Write Cycle



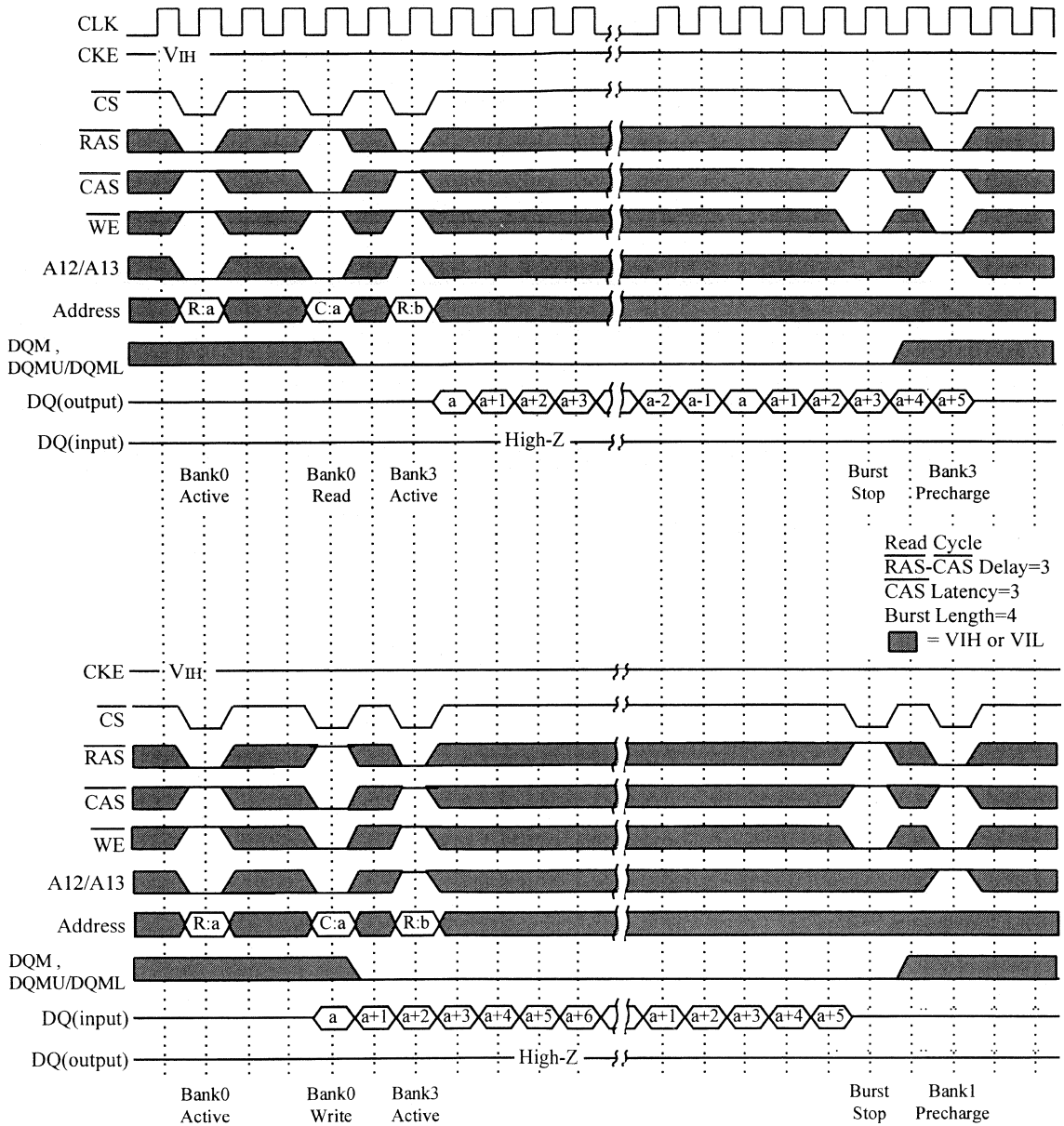
Read/Single Write Cycle
RAS-CAS Delay=3
CAS Latency=3
Burst Length=4
= VIH or VIL

Read / Burst Write Cycle

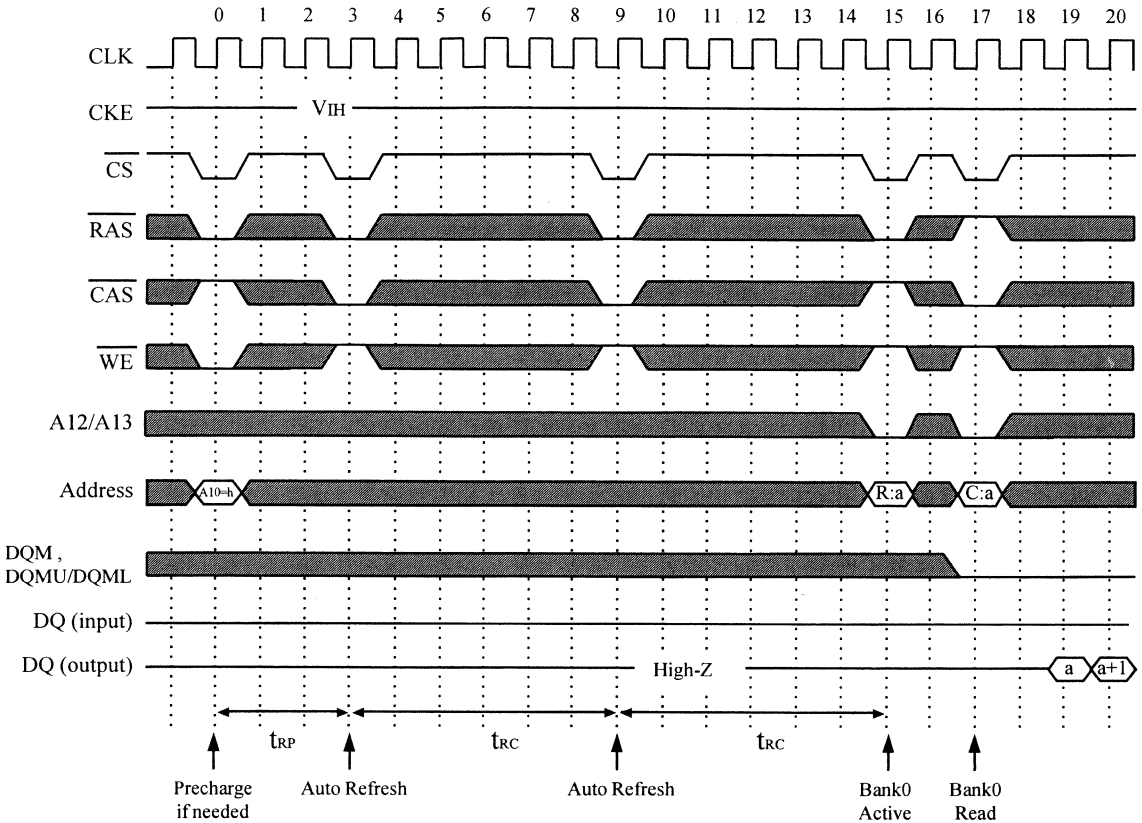


Read/Burst Write
RAS-CAS Delay=3
CAS Latency=3
Burst Length=4
▨ = VIH or VIL

Full Page Read / Write Cycle

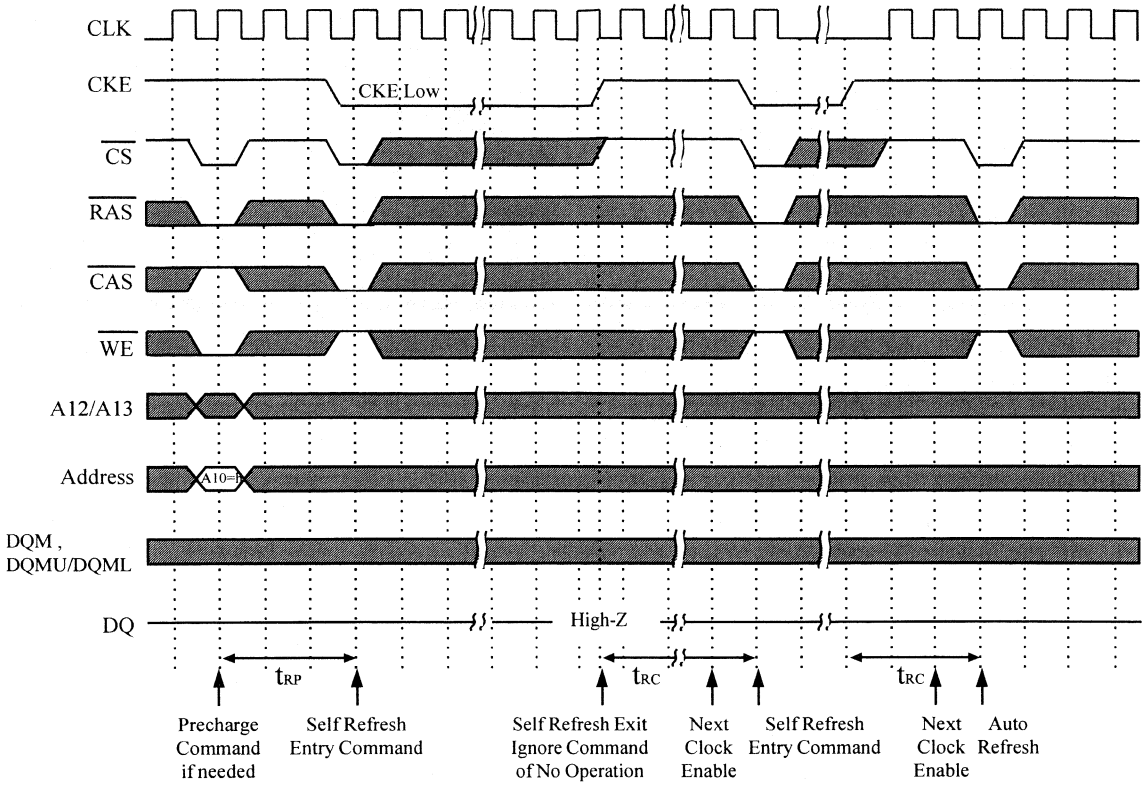


Auto Refresh Cycle



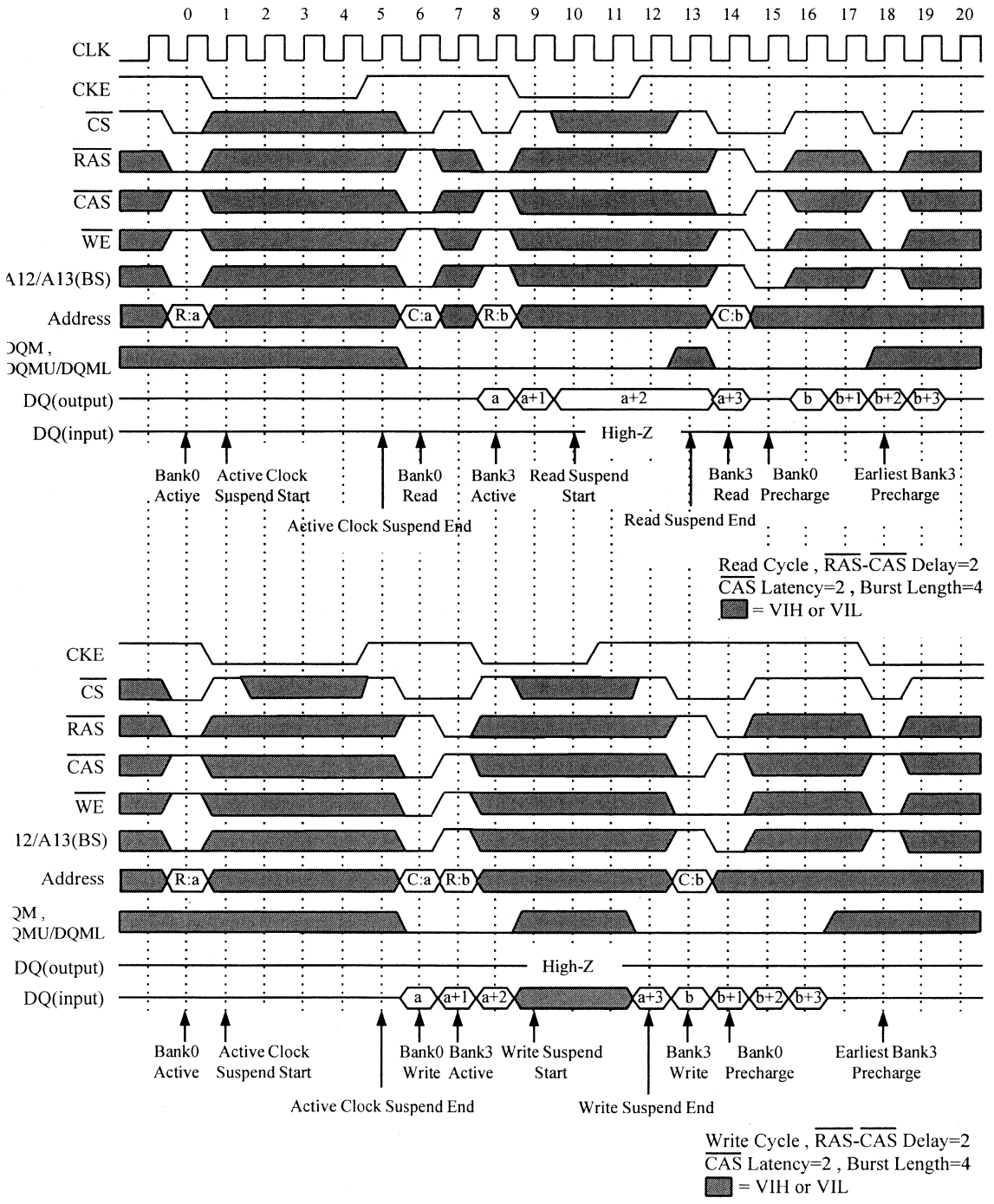
Refresh Cycle and
Read Cycle
RAS-CAS Delay=2
CAS Latency=2
Burst Length=4
= VIH or VIL

Self Refresh Cycle

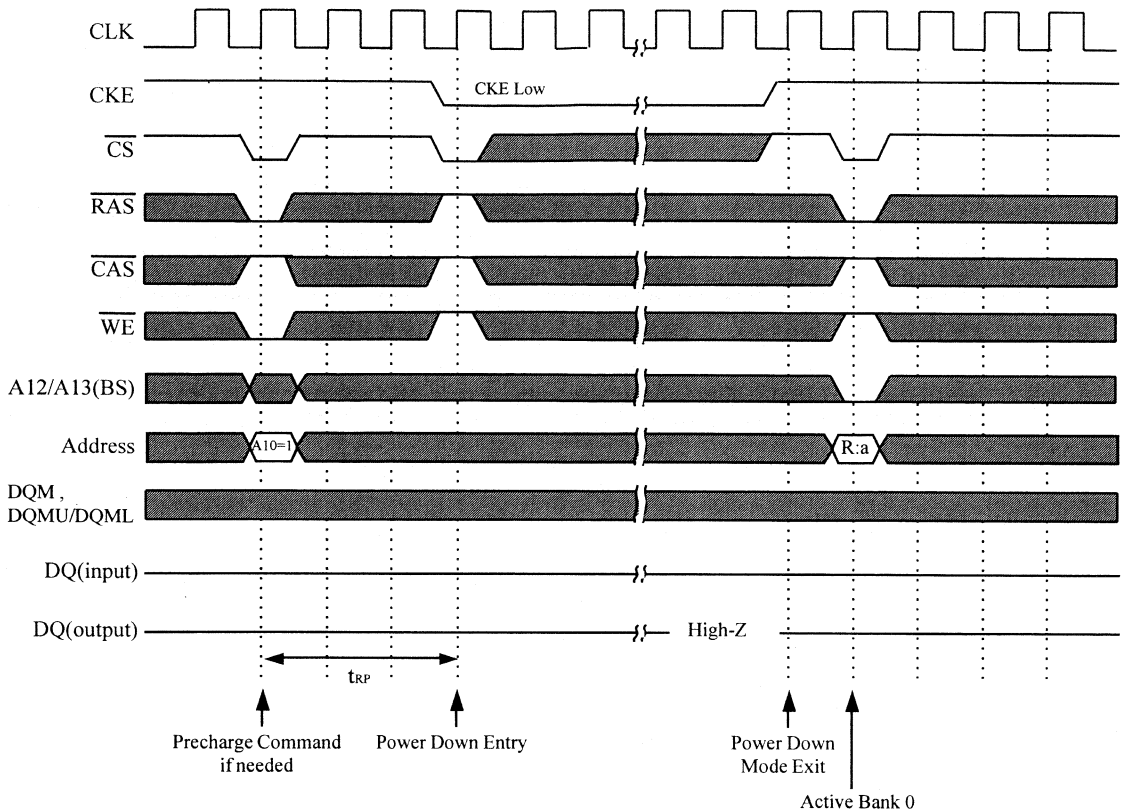


Self Refresh Cycle
RAS-CAS Delay = 3
CAS Latency=3
Burst Length=4
▨ = VIH or VIL

Clock Suspend (Active Power Down) Mode

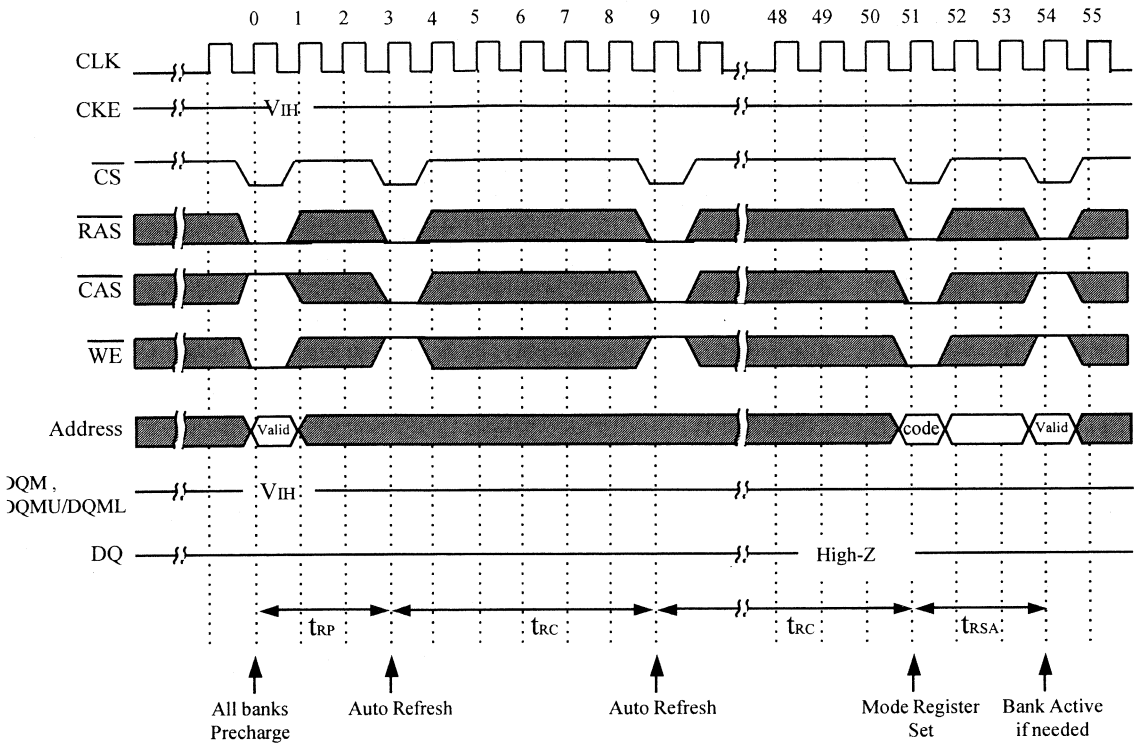


Power Down Mode



Powe Down Cycle
RAS-CAS Delay=3
CAS Latency=3
Burst Length=4
▨ = VIH or VIL

Power Up Sequence



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